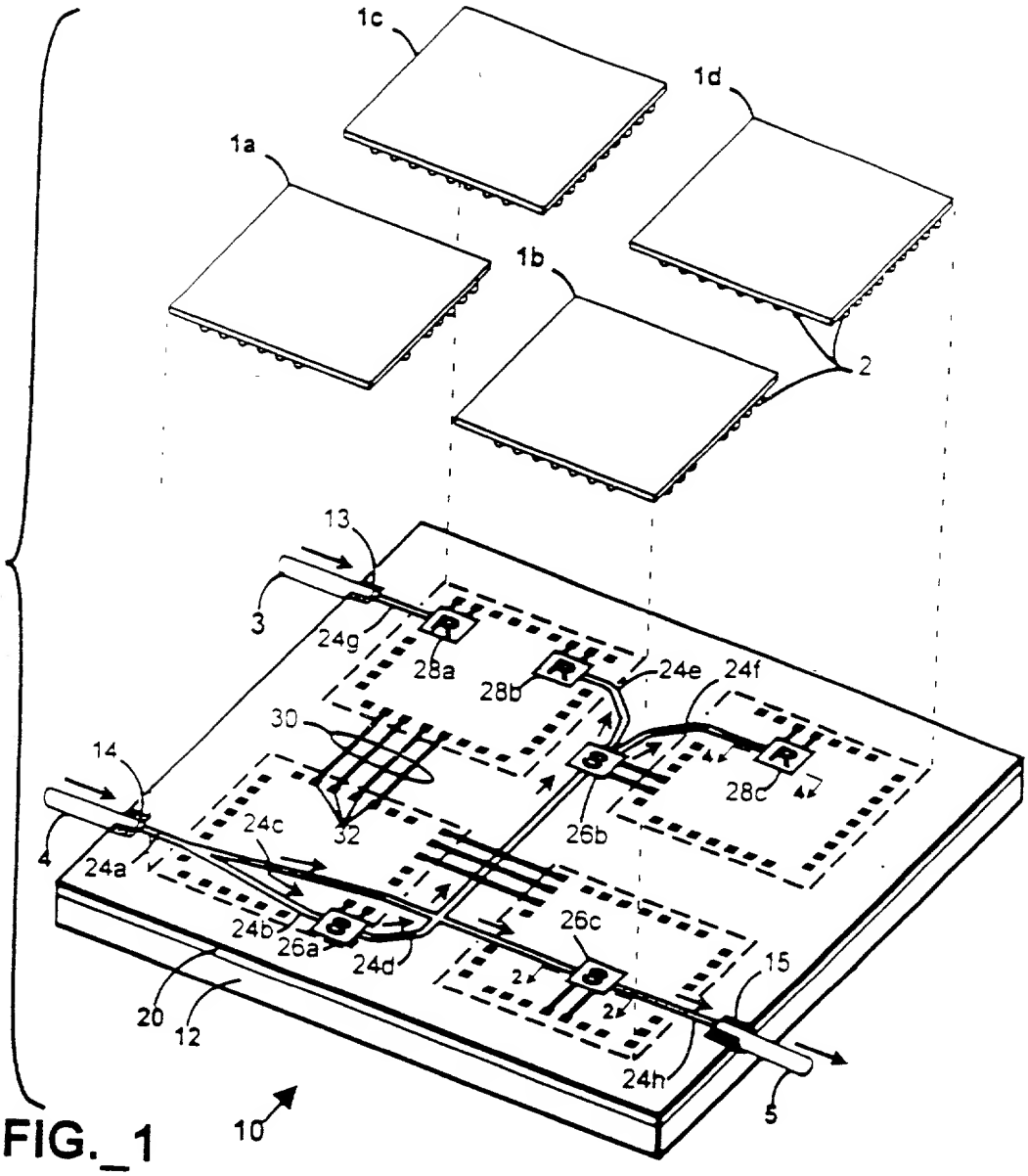

1c
1d
1a
1b
2
13
3
24g
28a
28b
24e
24f
30
14
28c
24c
32
26b
4
24a
24b
26a
24d
26c
15
20
12
24h
5
10

FIG._1

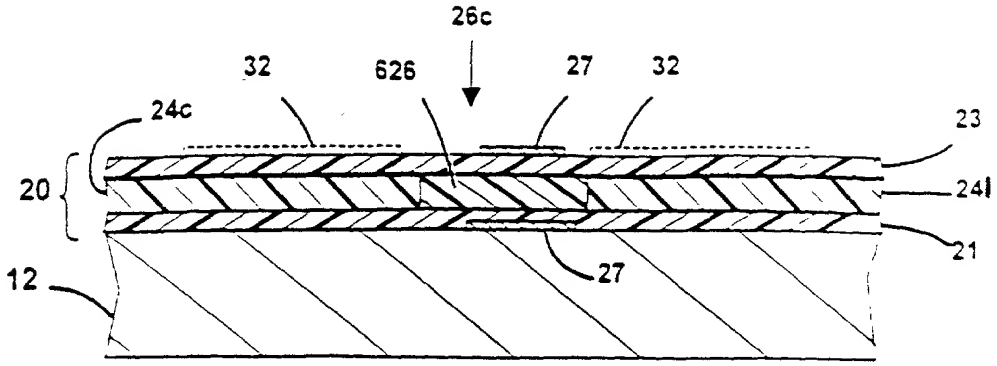

26c
32
626
27
32
24c
23
20
24i
21
27
12

FIG._2

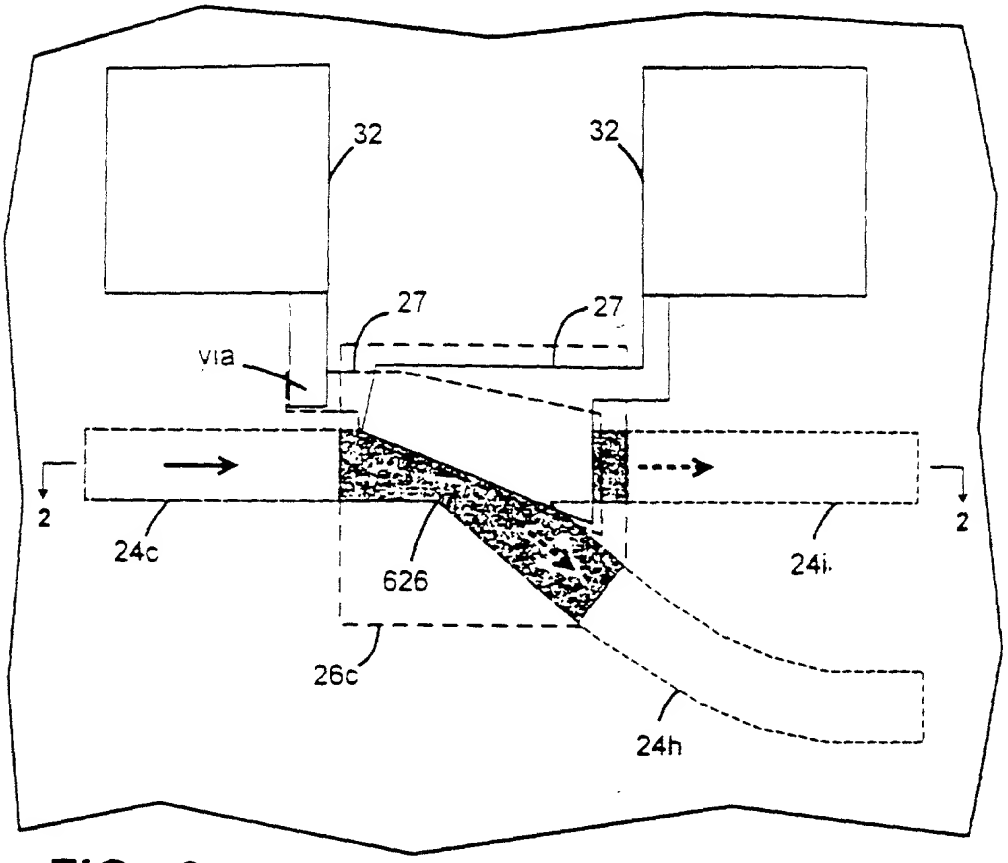

32
32
27
27
via
2
2
24c
626
24i
26c
24h

FIG._3

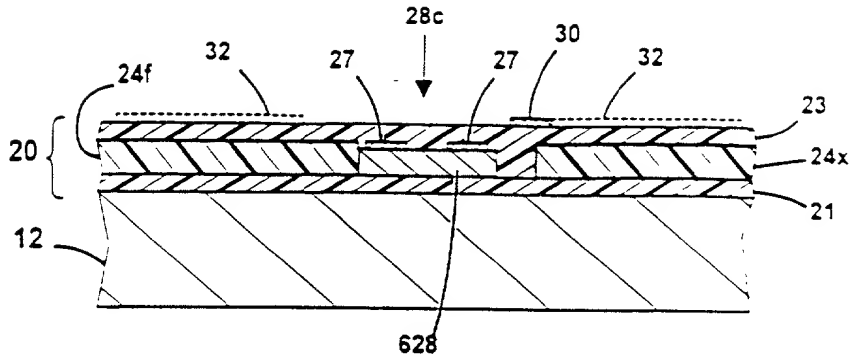

28c
32
27
27
30
32
24f
23
20
24x
21
12
628

FIG._4-1

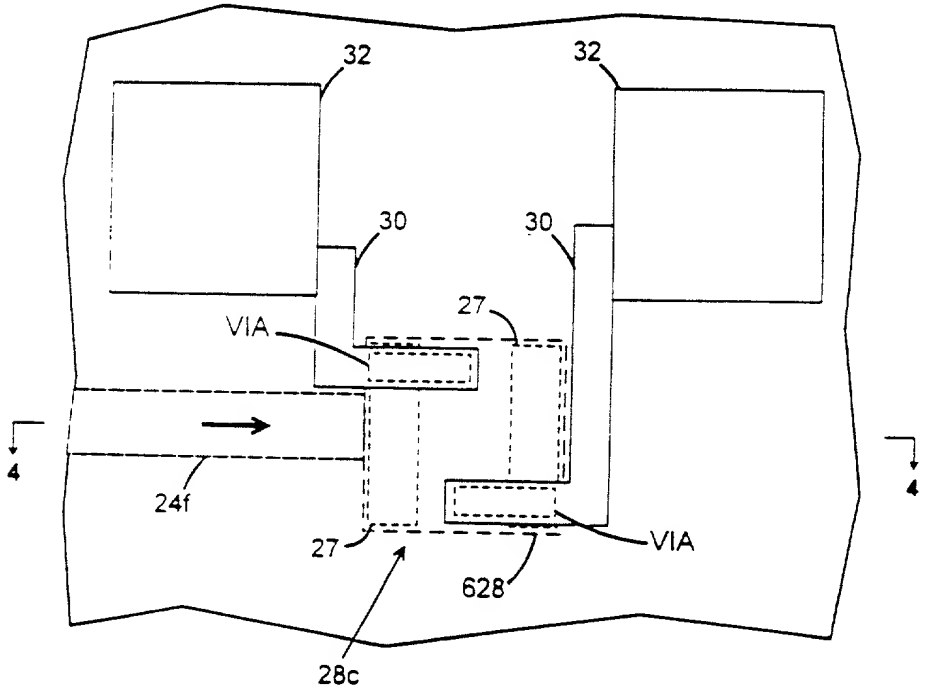

32
32
30
30
27
VIA
4
24f
27
VIA
628
28c
4

FIG._5-1

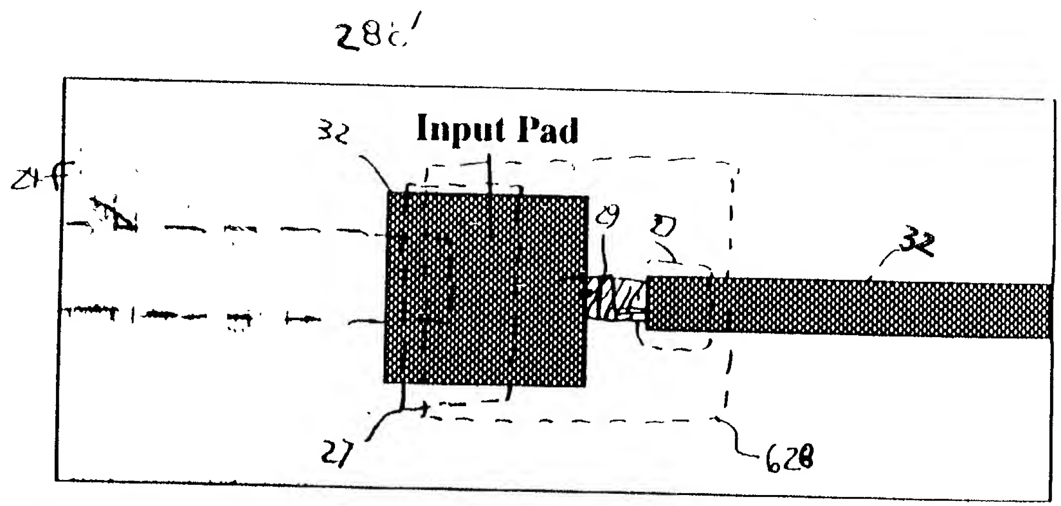

28c'
Input Pad
32
24f
29
27
62B

FIG. 5-2

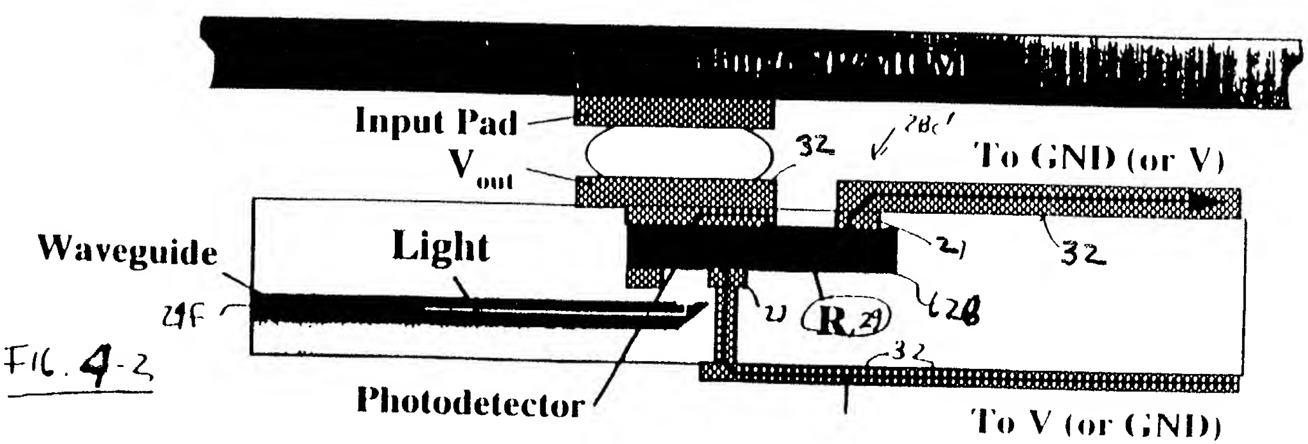

Input Pad
V out
32
28c'
To GND (or V)
Waveguide
Light
24f
21
R 29
62B
Photodetector
To V (or GND)

FIG. 4-2

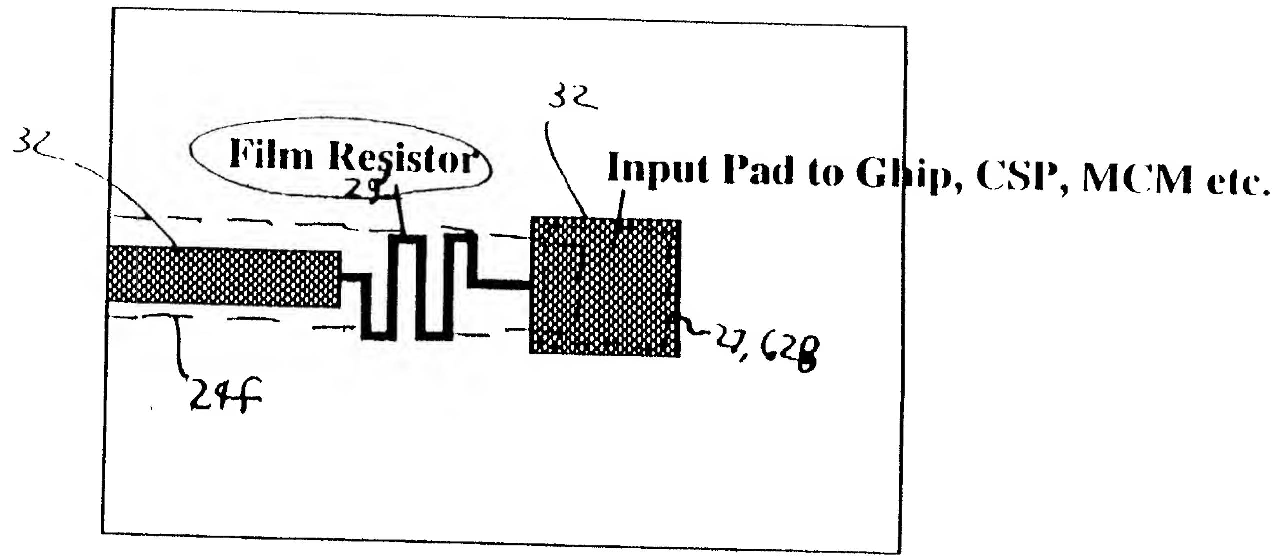

Film Resistor
29
32
32
Input Pad to Chip, CSP, MCM etc.
27, 628
24f

FIG. 5-3

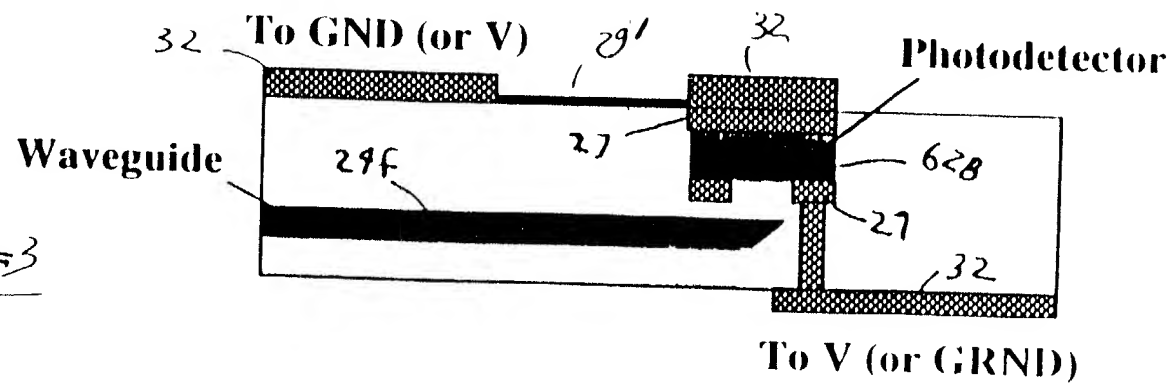

32
To GND (or V)
29'
32
Photodetector
Waveguide
24f
27
628
27
32
To V (or GRND)

FIG 4-3

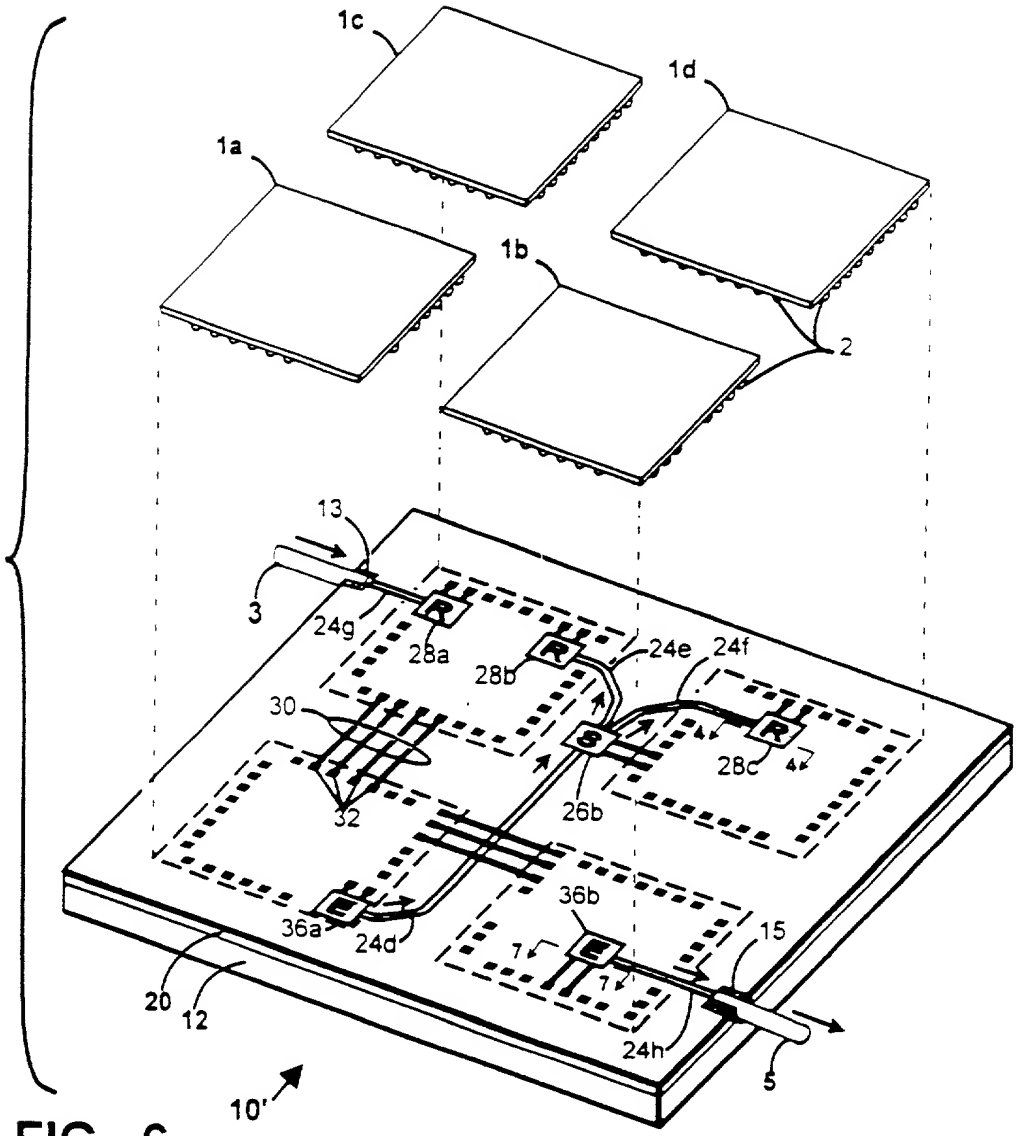

1c
1d
1a
1b
2
13
3
24g
28a
28b
24e
24f
30
28c
32
26b
36b
36a
24d
15
7
20
12
24h
5
10'

FIG._6

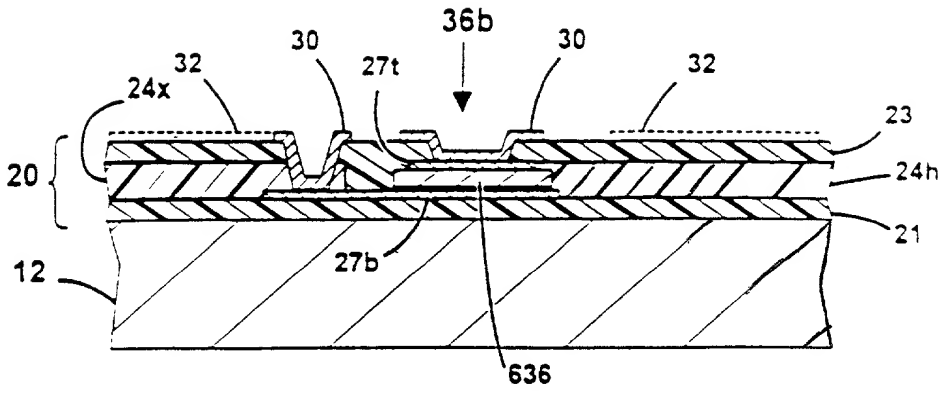

36b
30
30
32
32
27t
24x
23
20
24h
21
27b
12
636

FIG._7

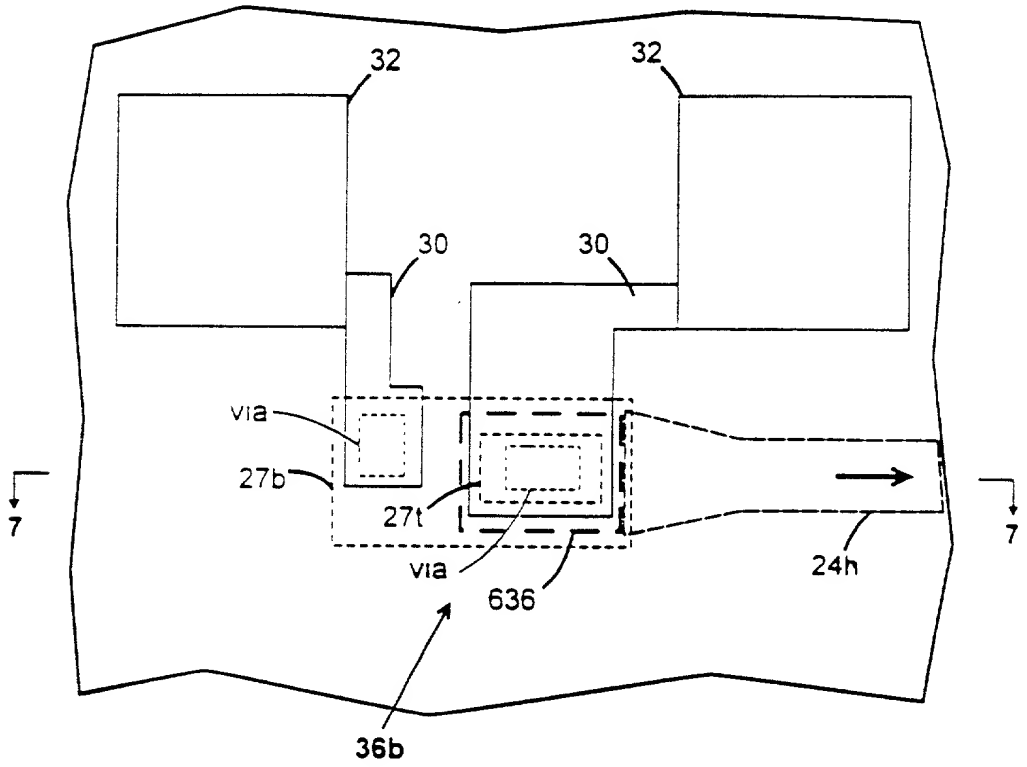

32
32
30
30
via
27b
27t
via
636
24h
7
7
36b

FIG._8

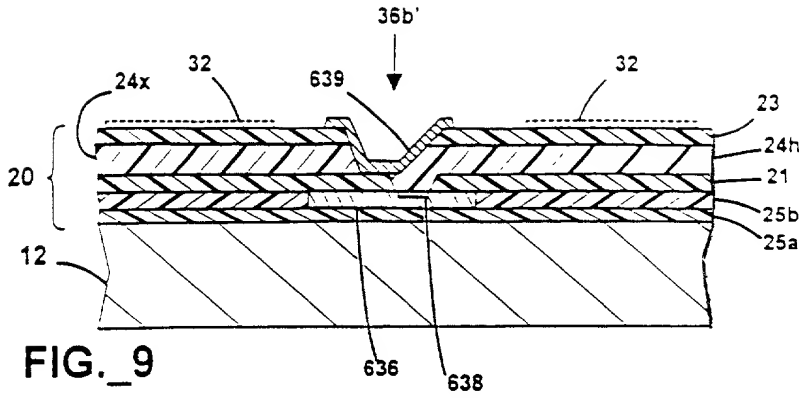

36b'
32
639
32
24x
23
24h
20
21
25b
25a
12
636
638

FIG._9

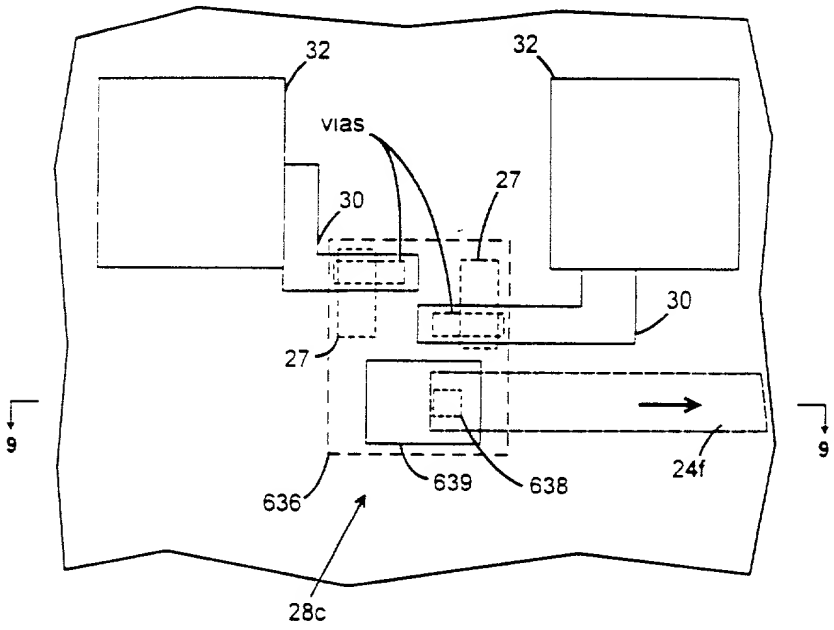

32
32
vias
27
30
30
27
9
9
24f
636
639
638
28c

FIG._10

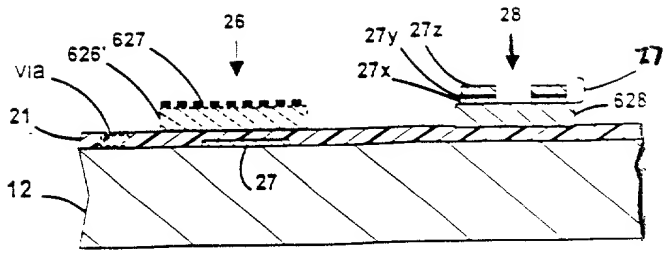


FIG._11

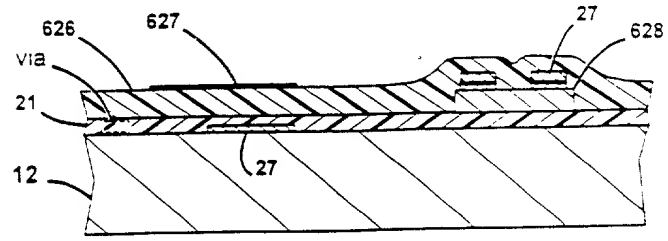


FIG._12

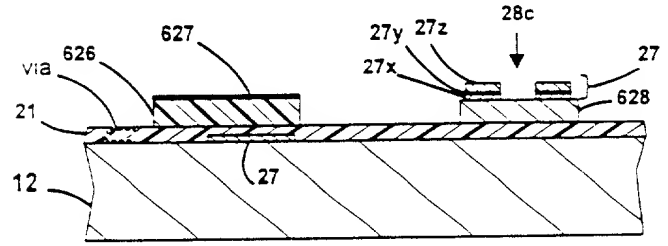


FIG._13

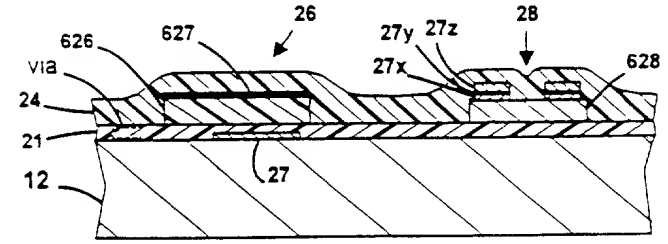


FIG._14

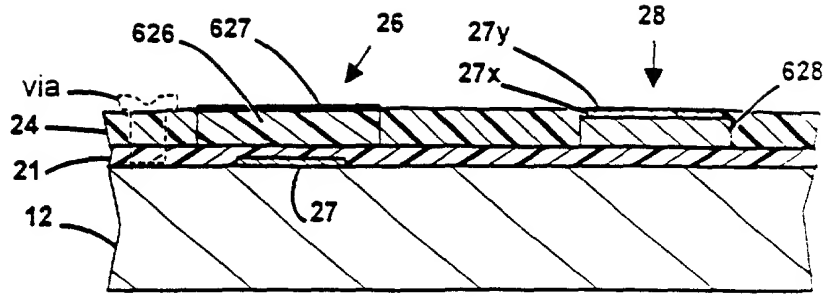


FIG._15

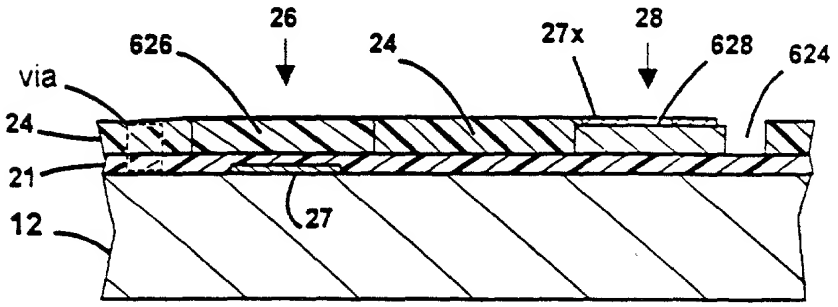


FIG._16

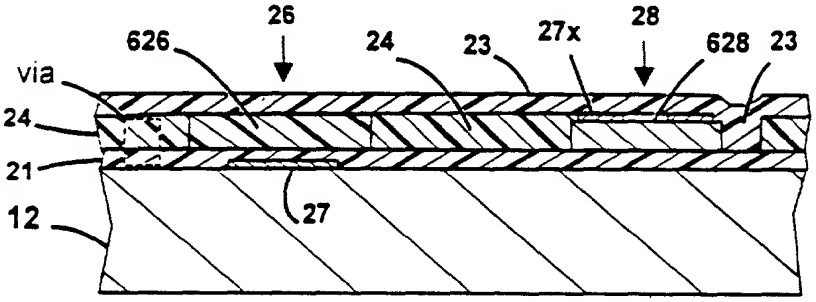


FIG._17

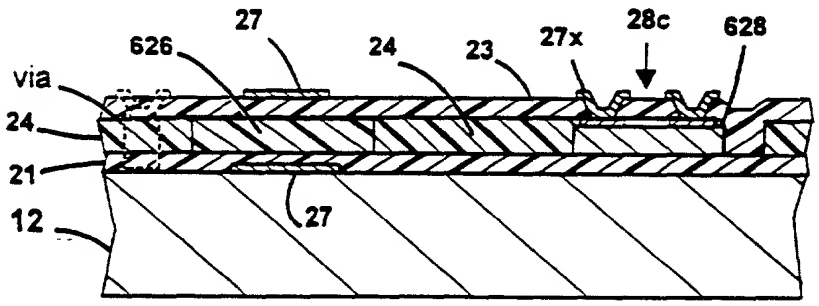


FIG._18

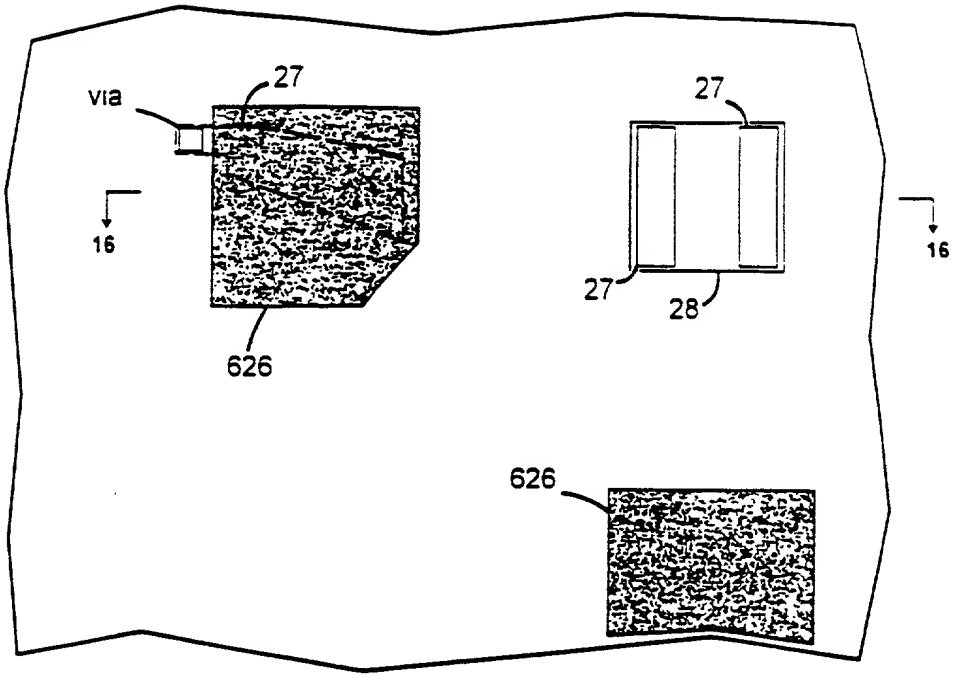

via
27
16
626
27
27
28
16
626

FIG._19

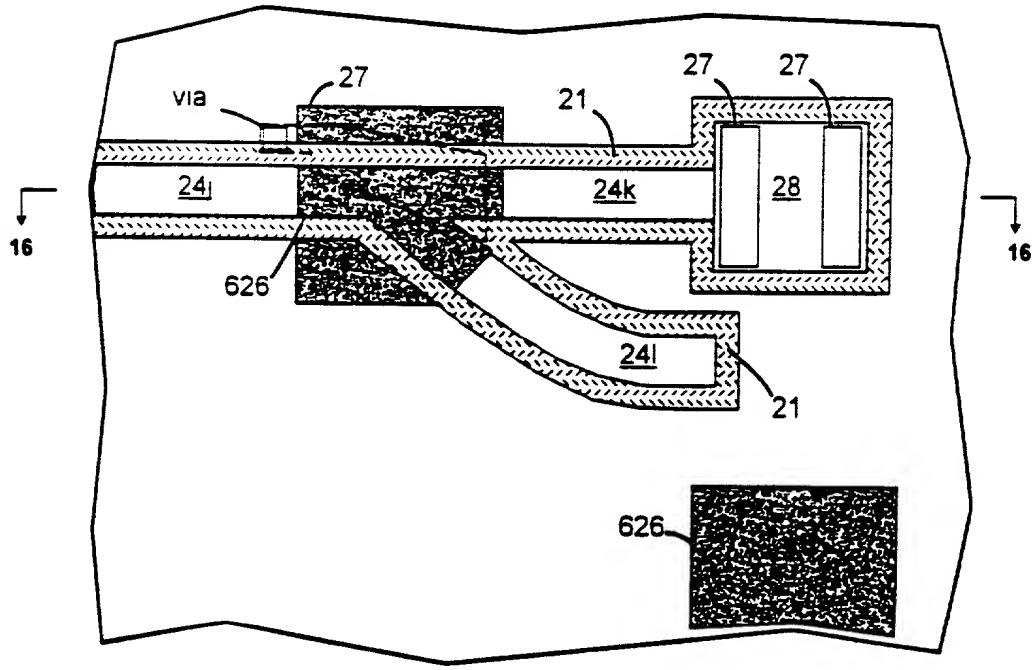

via
27
21
27
27
24j
24k
28
16
626
24l
21
16
626

FIG._20

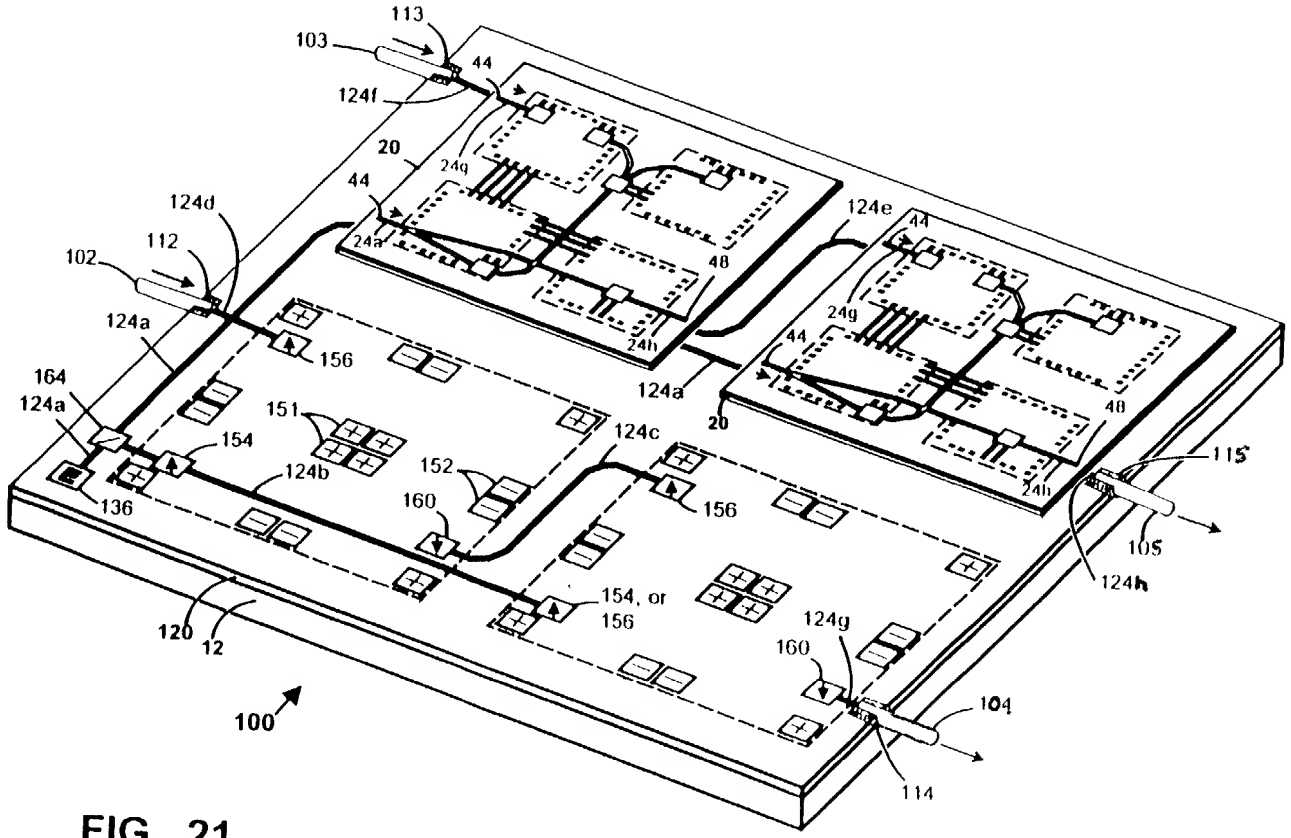

113
103
44
124f
20
24g
44
124d
112
102
24a
48
124e
44
24g
124a
156
44
24h
164
124a
151
124a
20
154
124c
115
124b
152
156
136
160
105
124h
154, or
156
120
12
124g
160
104
100
114

FIG._21

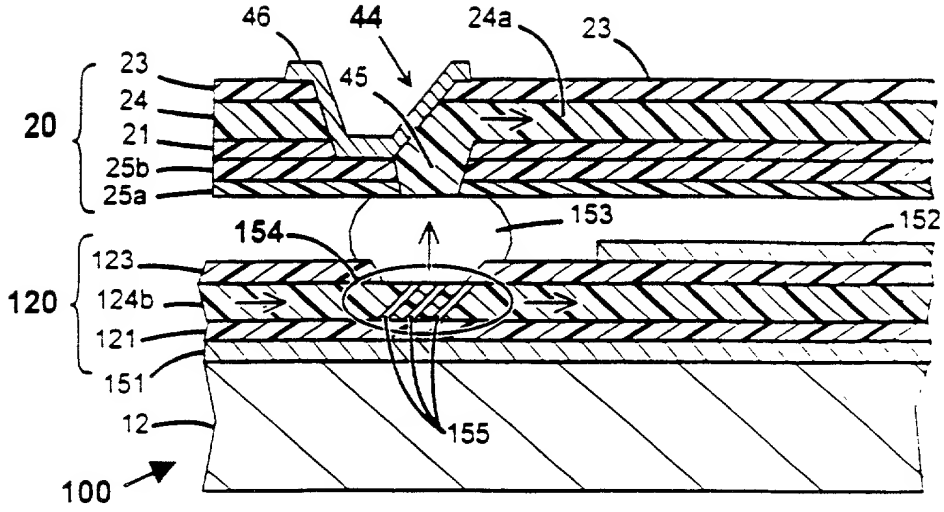

46
44
24a
23
45
23
24
21
20
25b
25a
153
152
154
123
124b
120
121
151
12
155
100

FIG._22

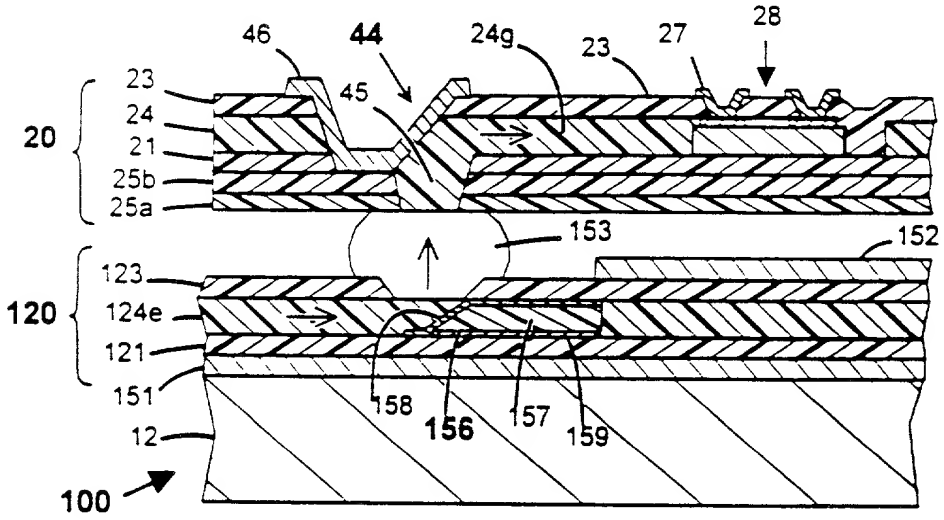

46
44
24g
23
27
28
45
23
24
21
20
25b
25a
153
152
123
124e
120
121
151
158
156
157
159
12
100

FIG._23

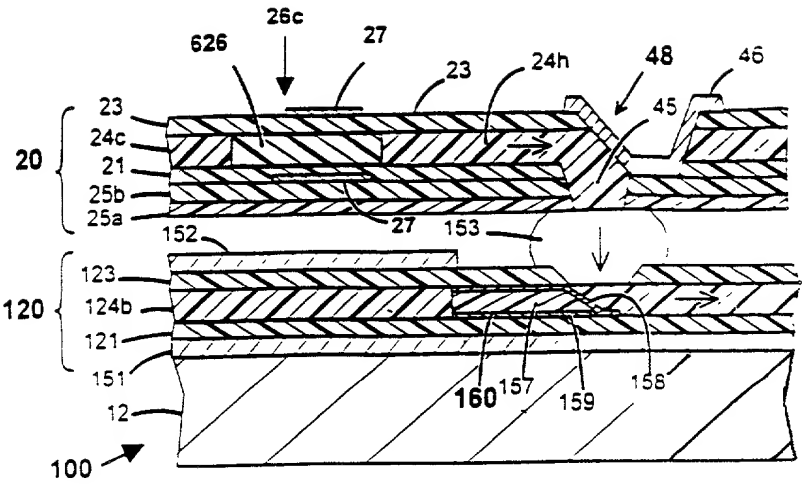


FIG._24

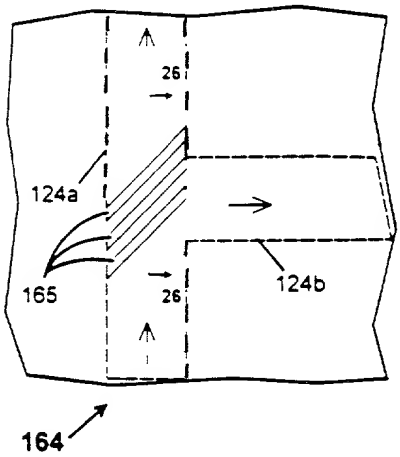


FIG._25

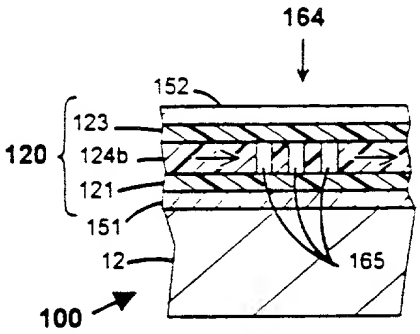


FIG._26

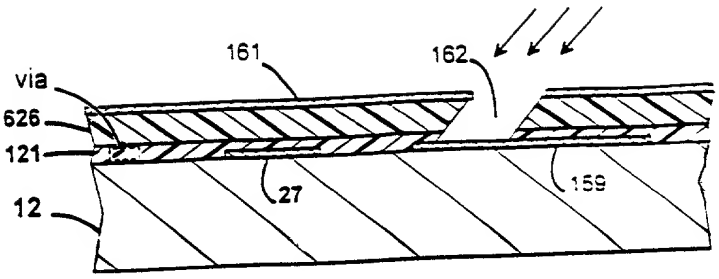


FIG._27

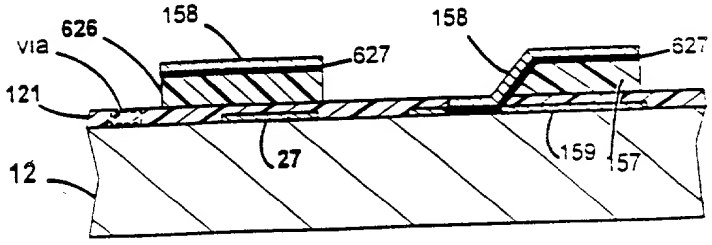


FIG._28

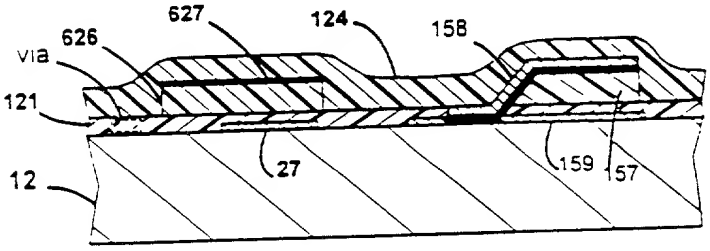


FIG._29

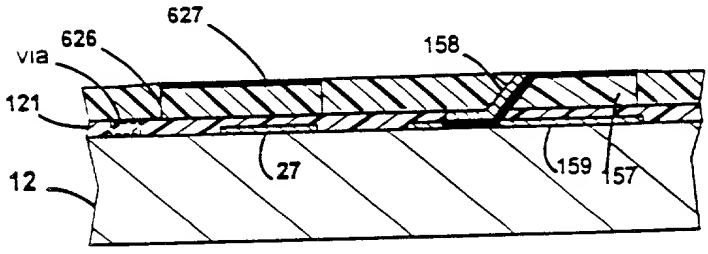


FIG._30

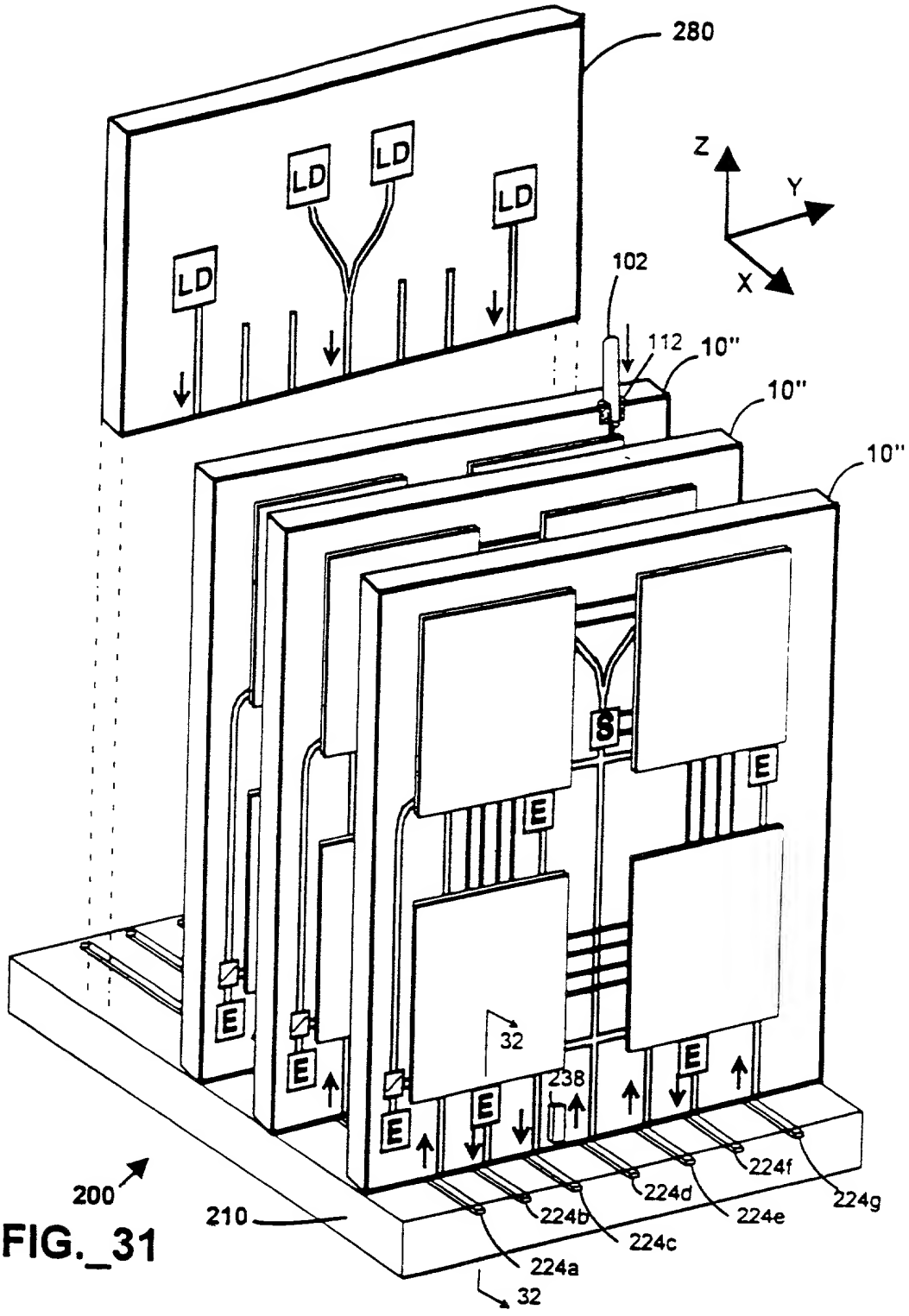

280
LD
LD
LD
LD
Z
Y
X
102
112
10"
10"
10"
S
E
E
E
E
E
E
E
E
32
238
200
210
224a
224b
224c
224d
224e
224f
224g
32

FIG._31

FIG._32

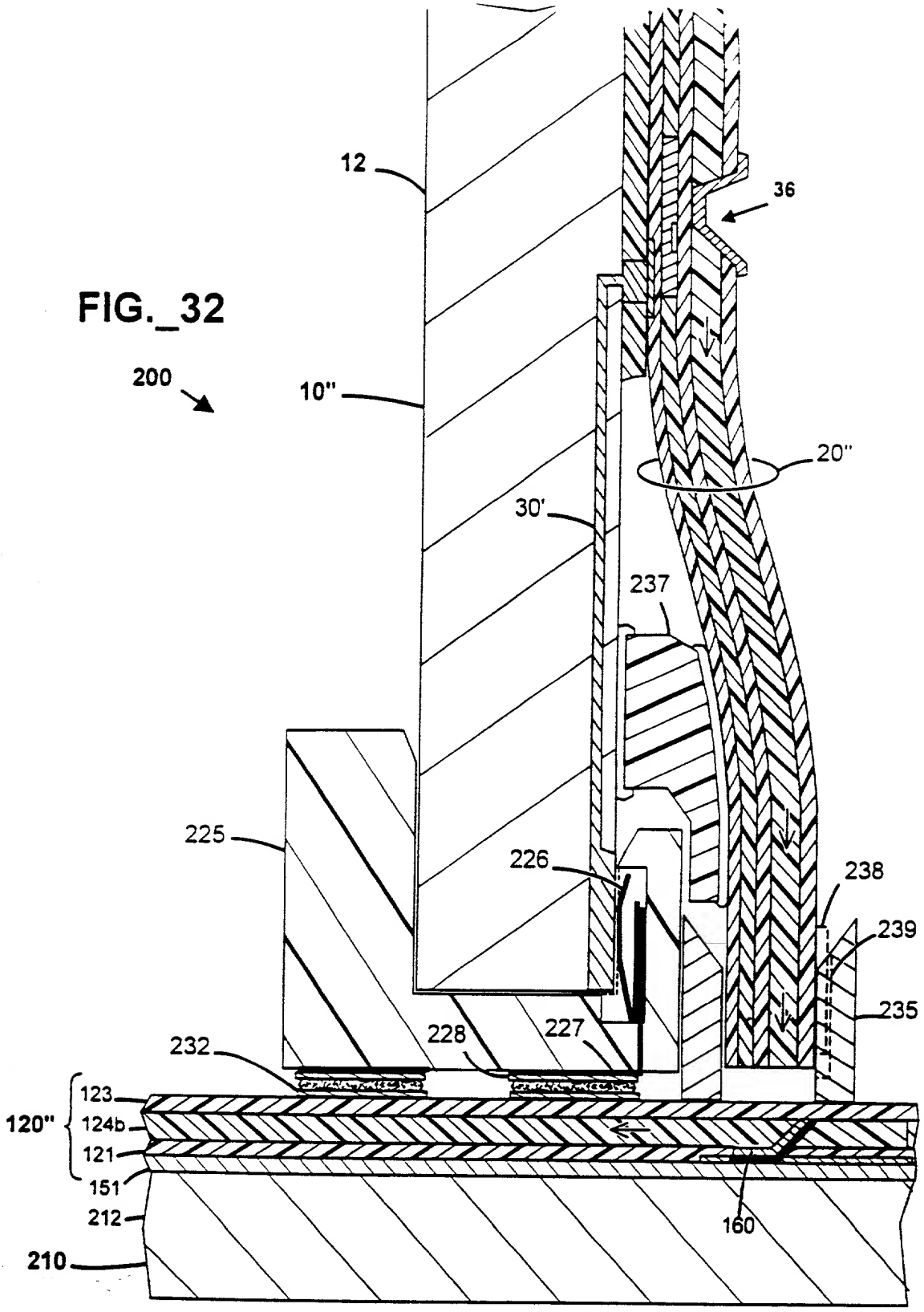
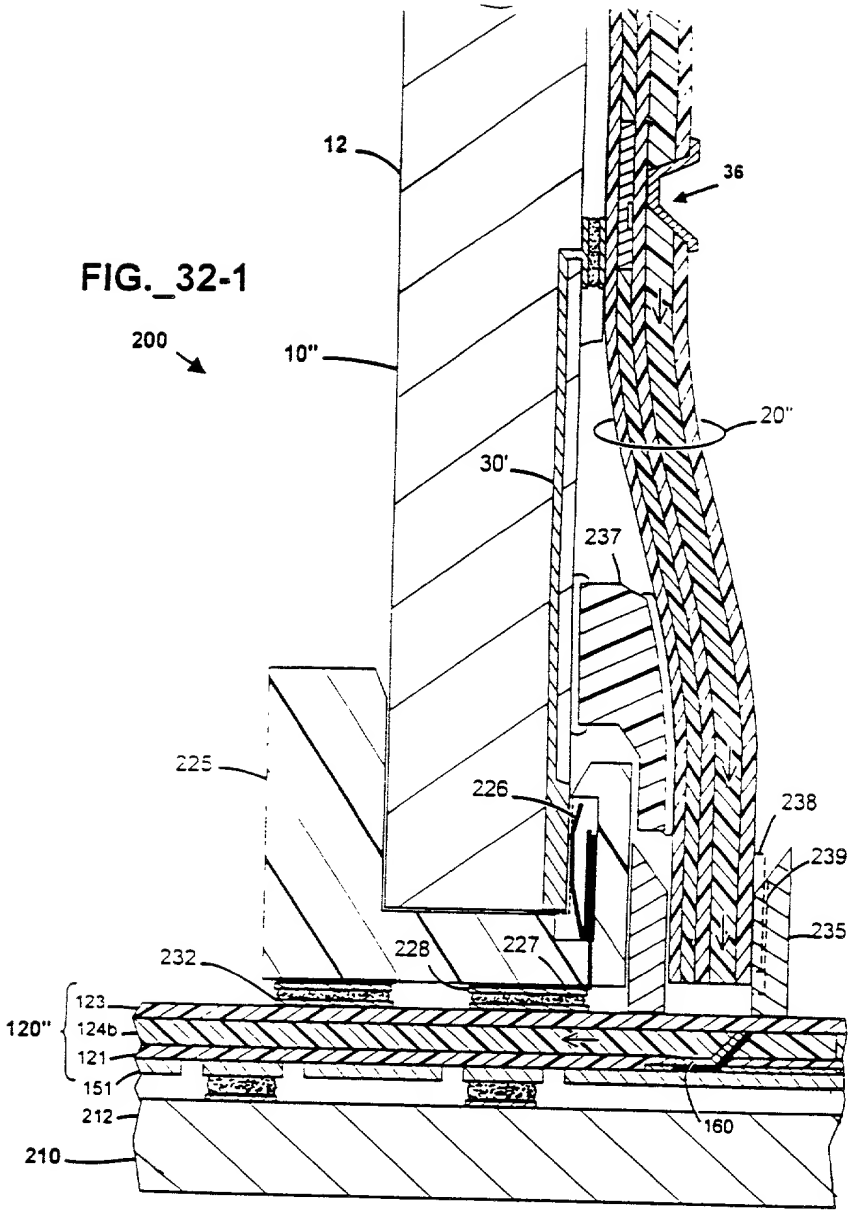

200
12
36
10"
20"
30'
237
225
226
238
239
235
228
227
232
120"
123
124b
121
151
212
210
160

FIG._32-1


200
12
36
10"
20"
30'
237
225
226
238
239
235
232
228
227
120"
123
124b
121
151
212
210
160

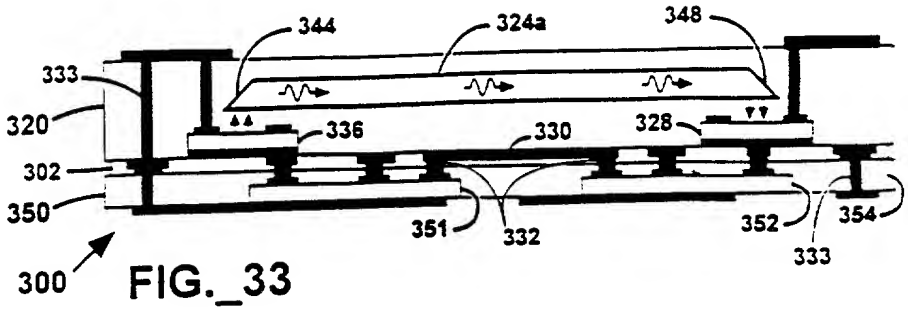


FIG._33

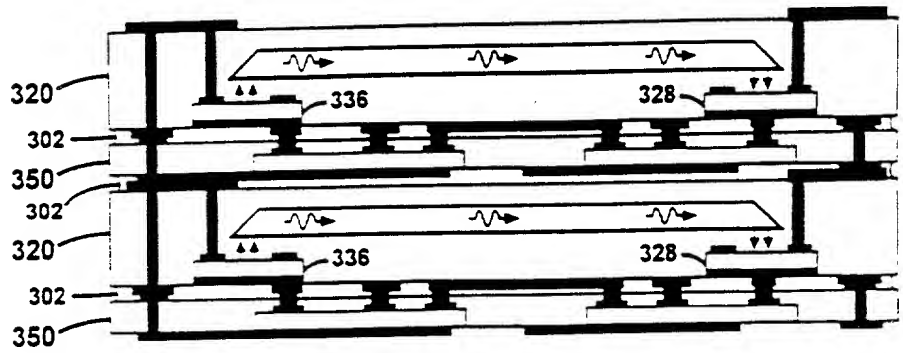


FIG._34

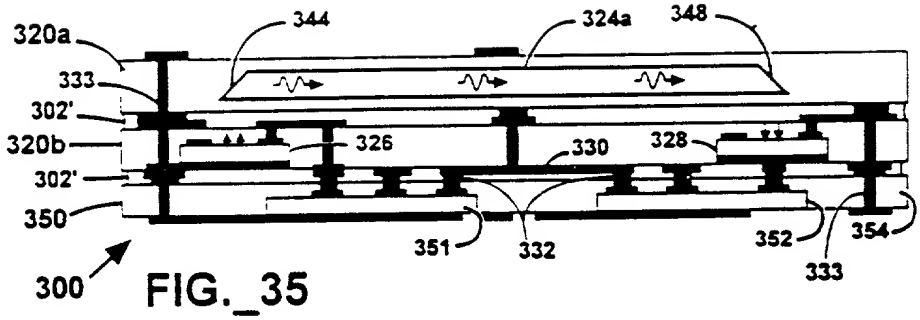


FIG._35

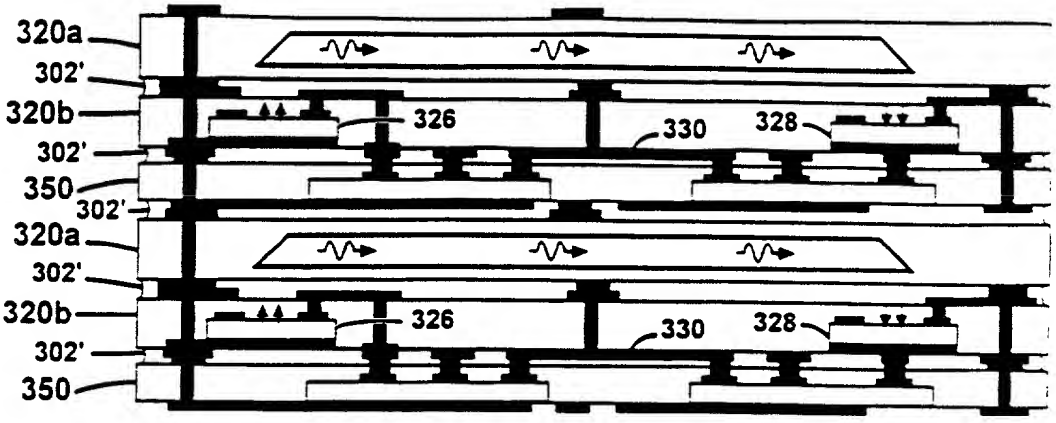


FIG._36

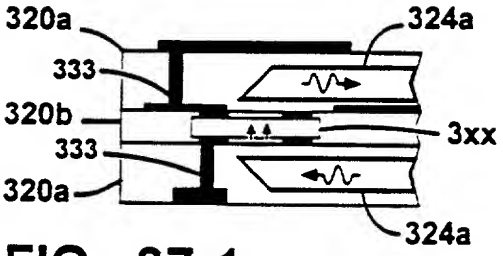


FIG._37-1

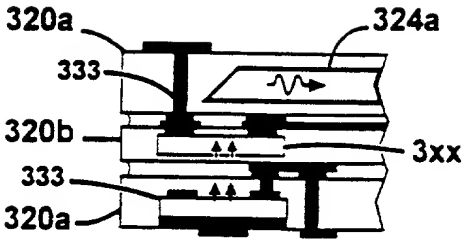


FIG._37-2

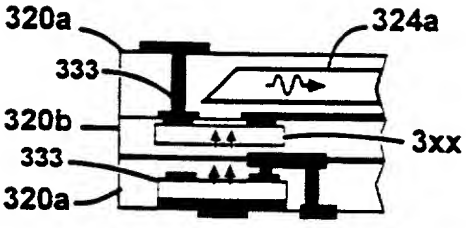


FIG._37-3

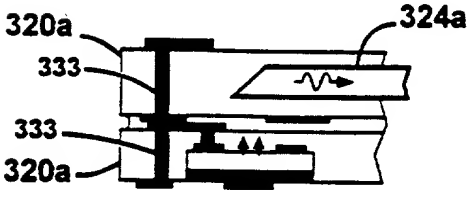


FIG._37-4

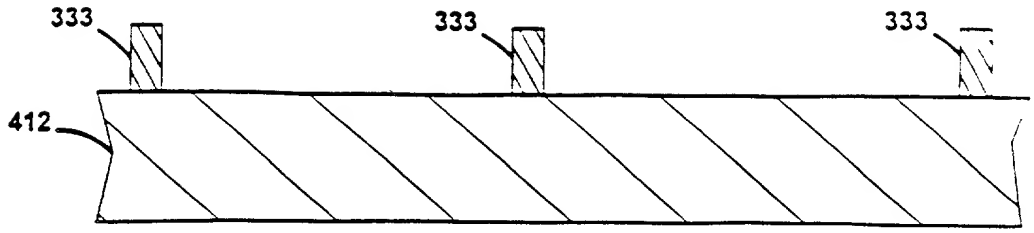


FIG._38

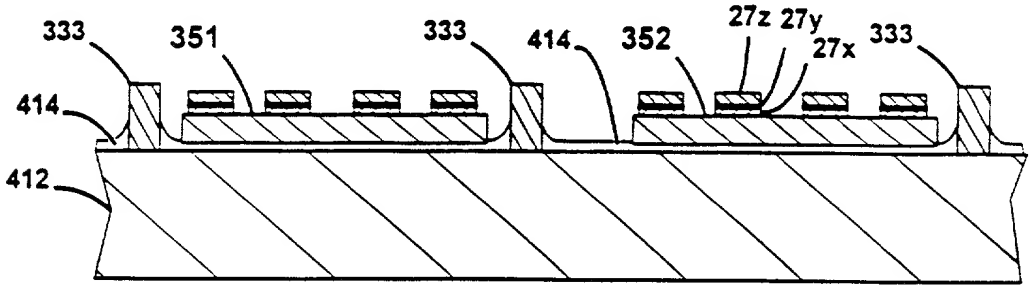


FIG._39

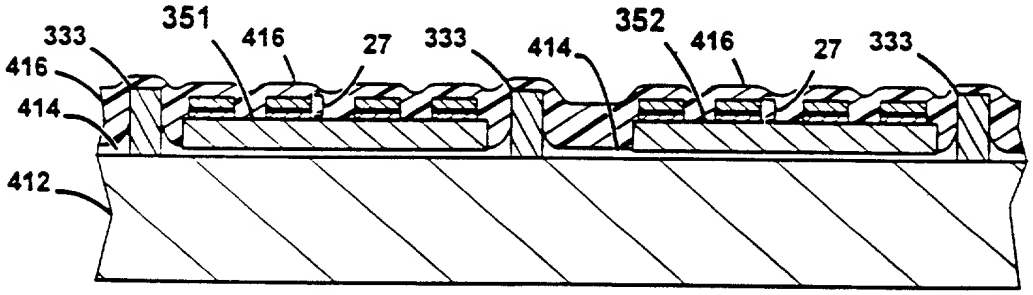


FIG._40

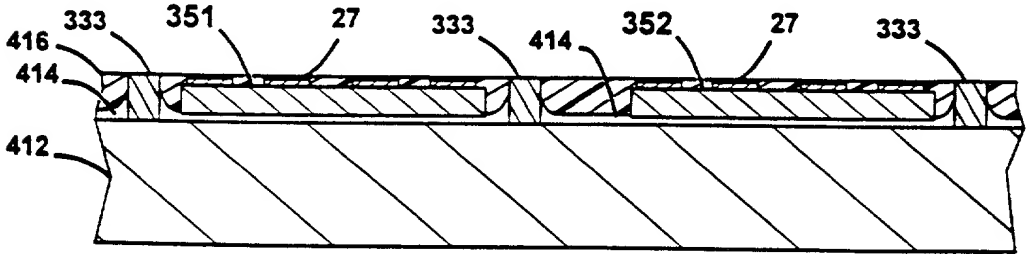


FIG._41

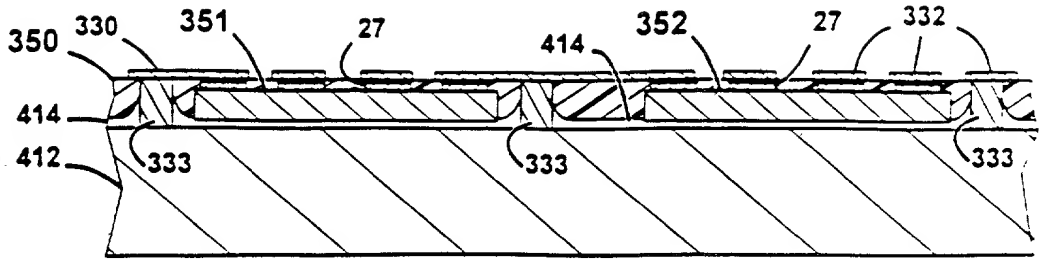


FIG._42

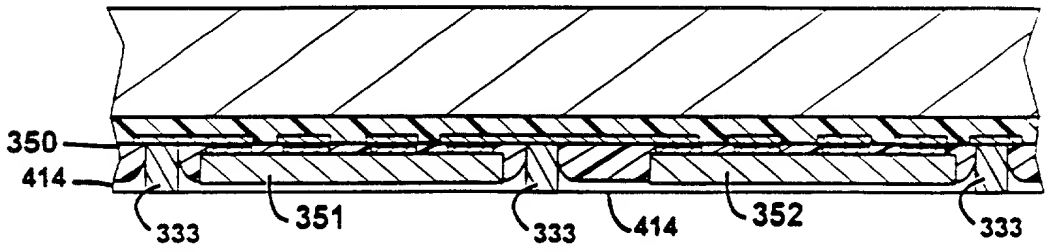


FIG._43

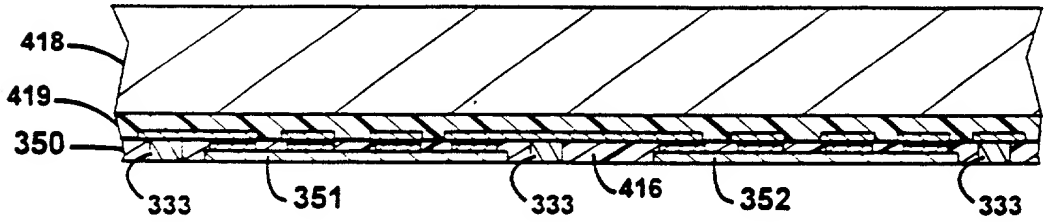


FIG._44

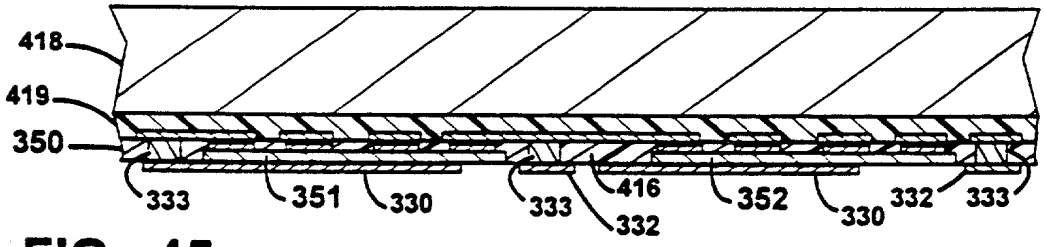


FIG._45

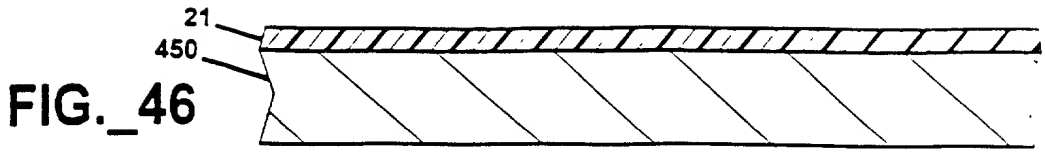


FIG._46

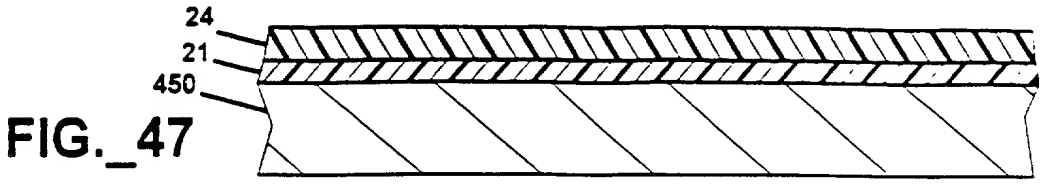


FIG._47

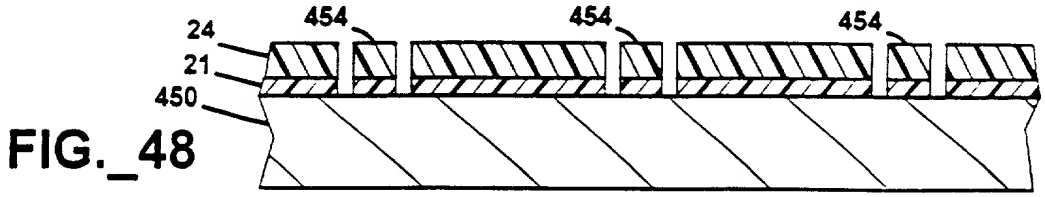


FIG._48

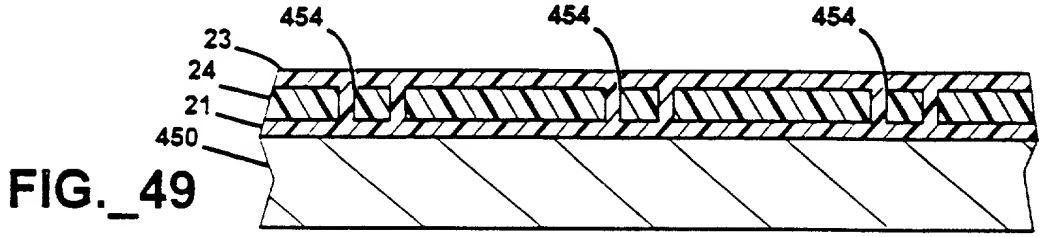


FIG._49

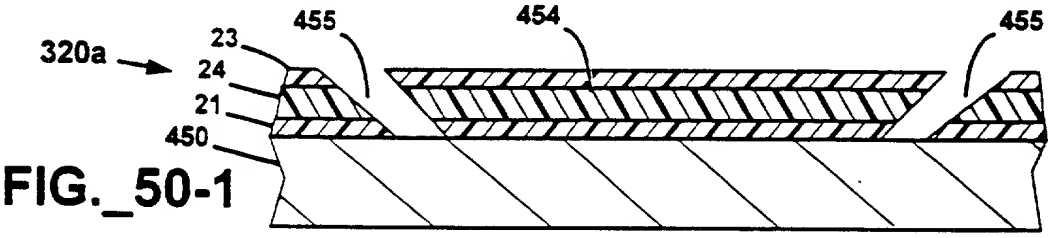


FIG._50-1

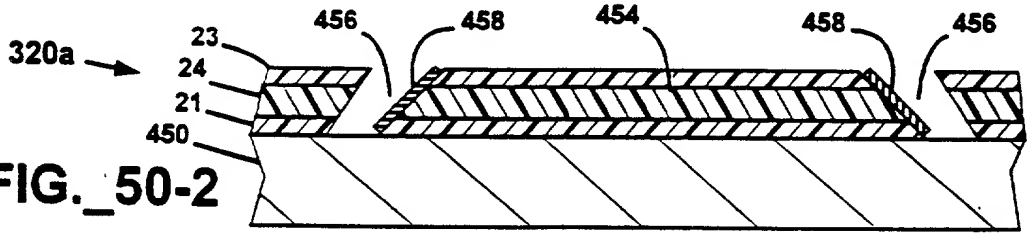


FIG._50-2

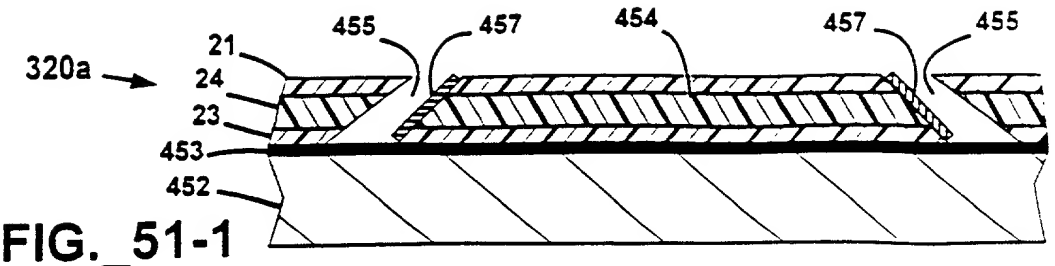


FIG._51-1

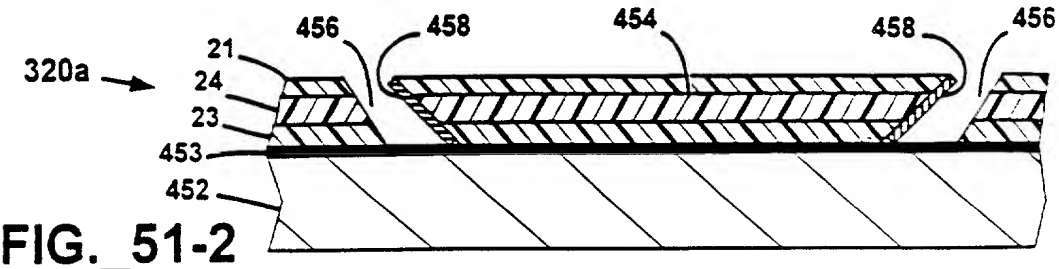


FIG._51-2

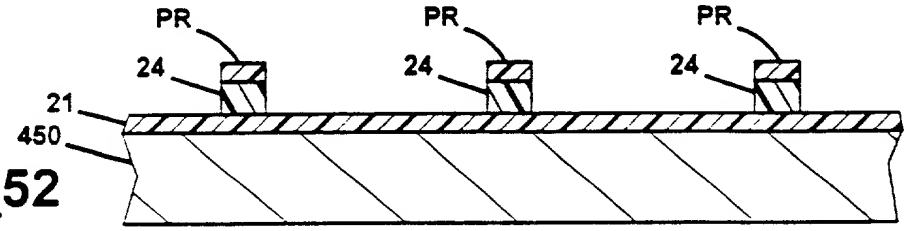


FIG._52

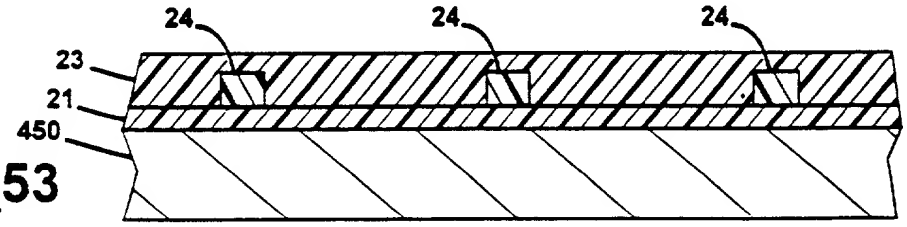


FIG._53

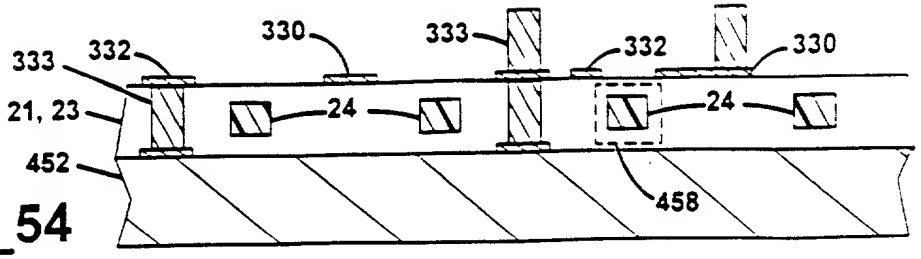


FIG._54

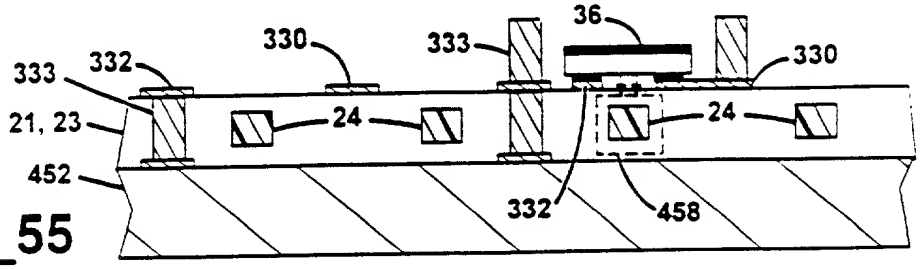


FIG._55

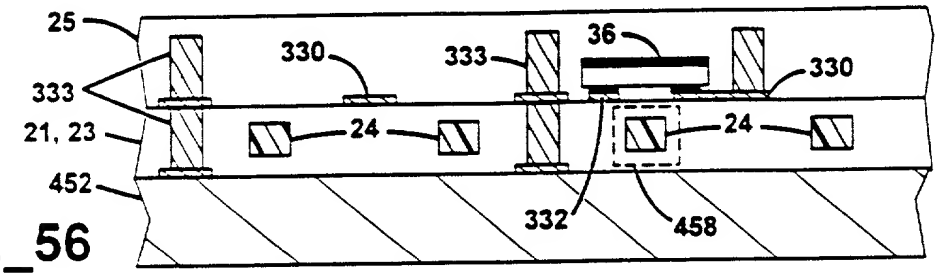


FIG._56

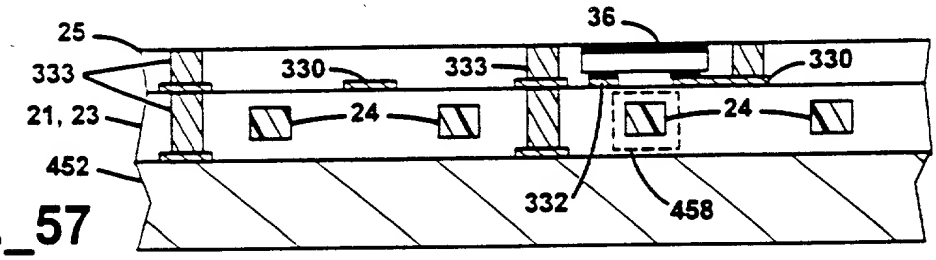


FIG._57

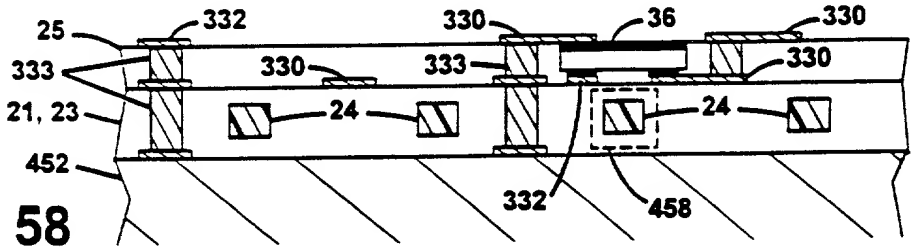


FIG. 58

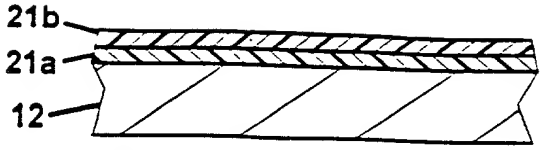


FIG._59

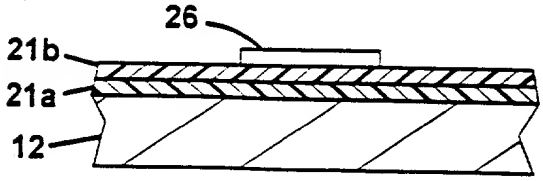


FIG._60

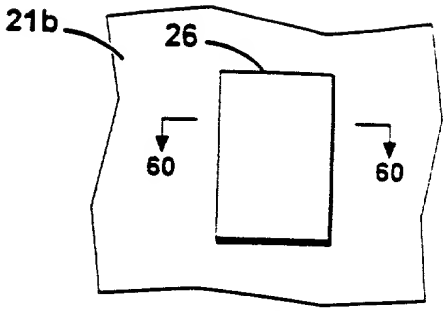


FIG._61

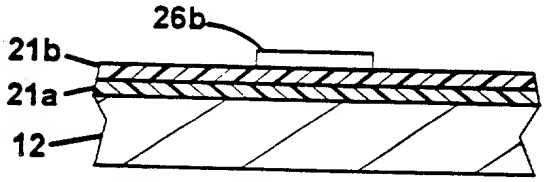


FIG._62

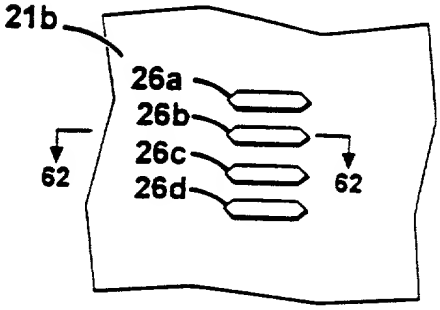


FIG._63

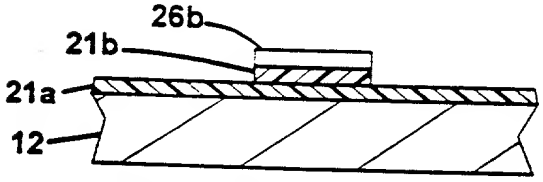


FIG._64

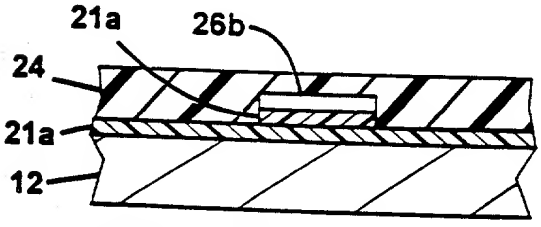


FIG._65

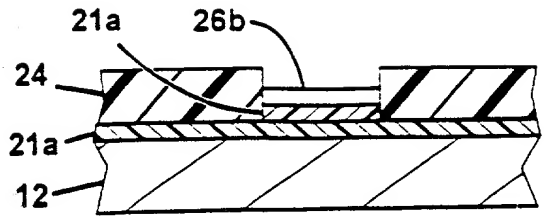


FIG._66

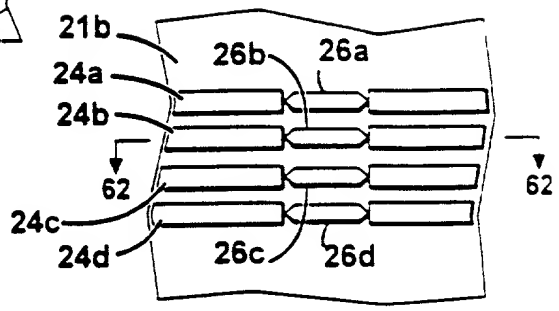


FIG._67

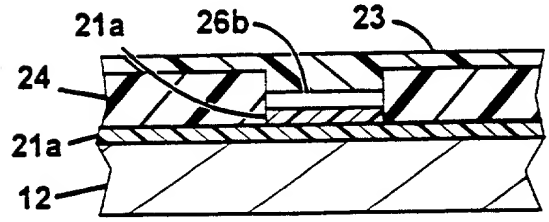


FIG._68

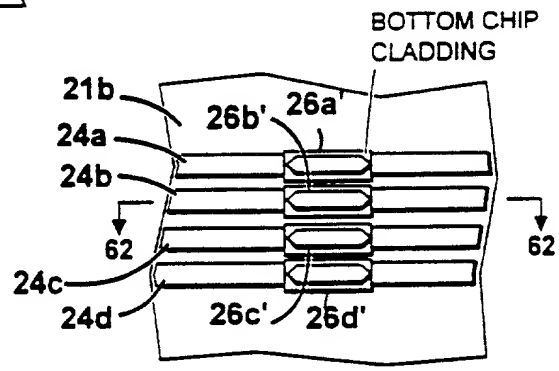
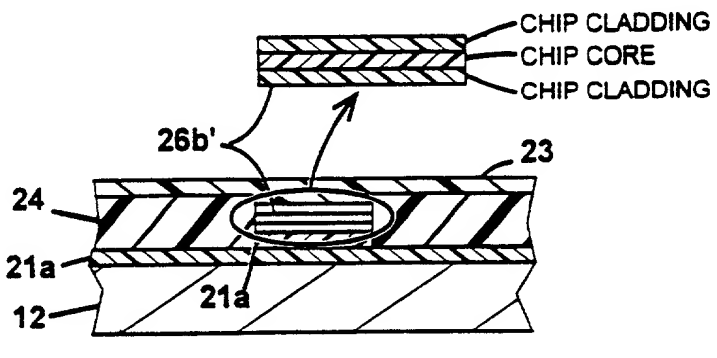


FIG._67-2

FIG._68-2



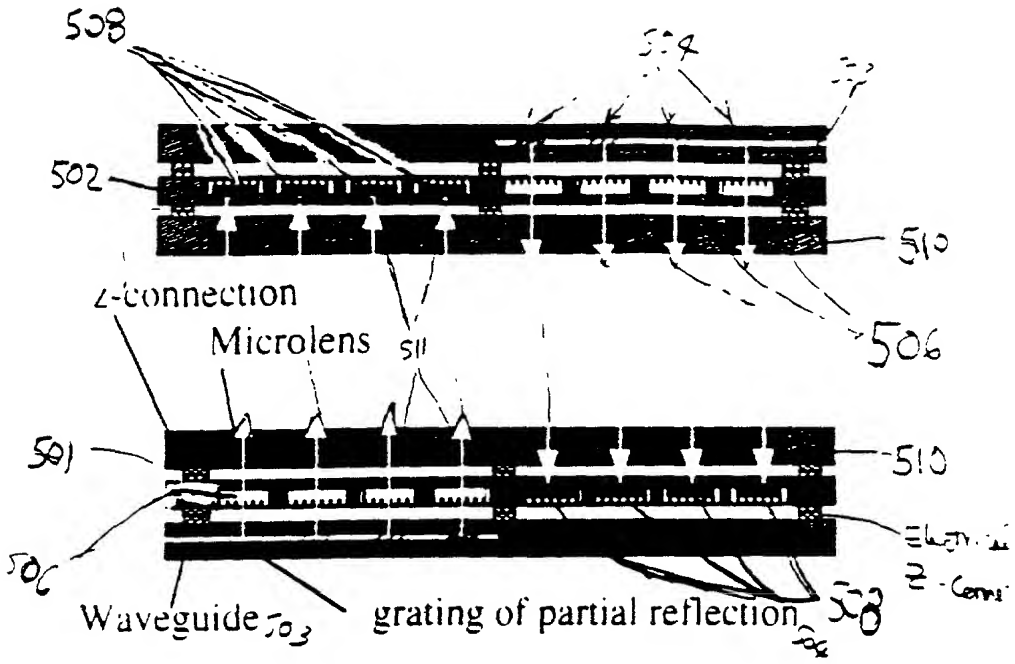

508
502
510
506
Microlens
511
501
510
Waveguide
grating of partial reflection

FIG. 69

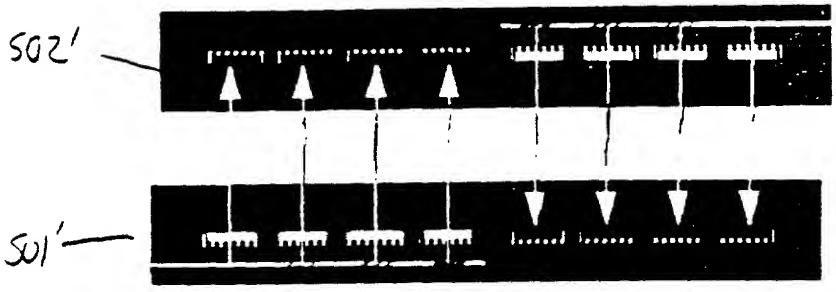

502'
501'

FIG. 70

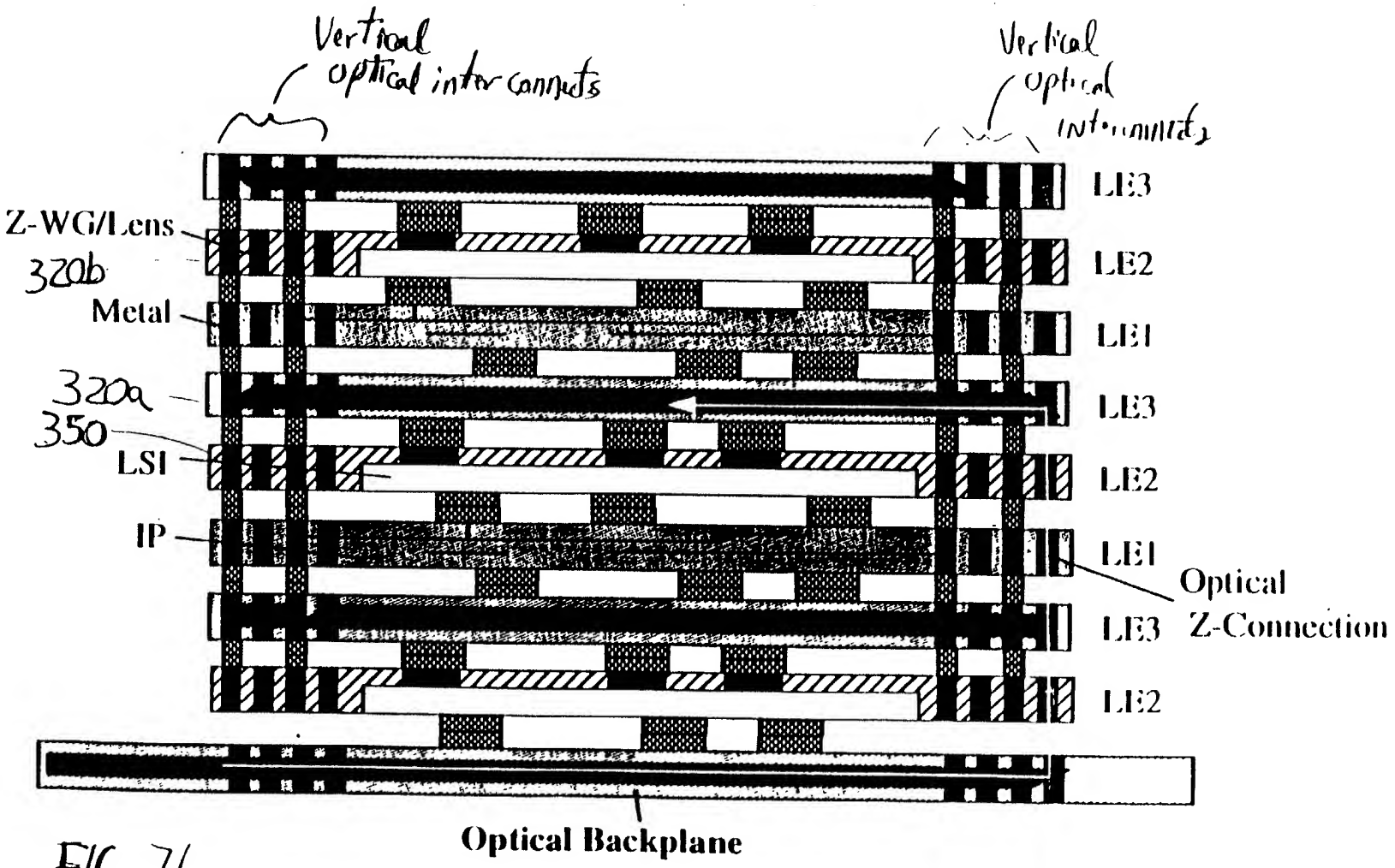
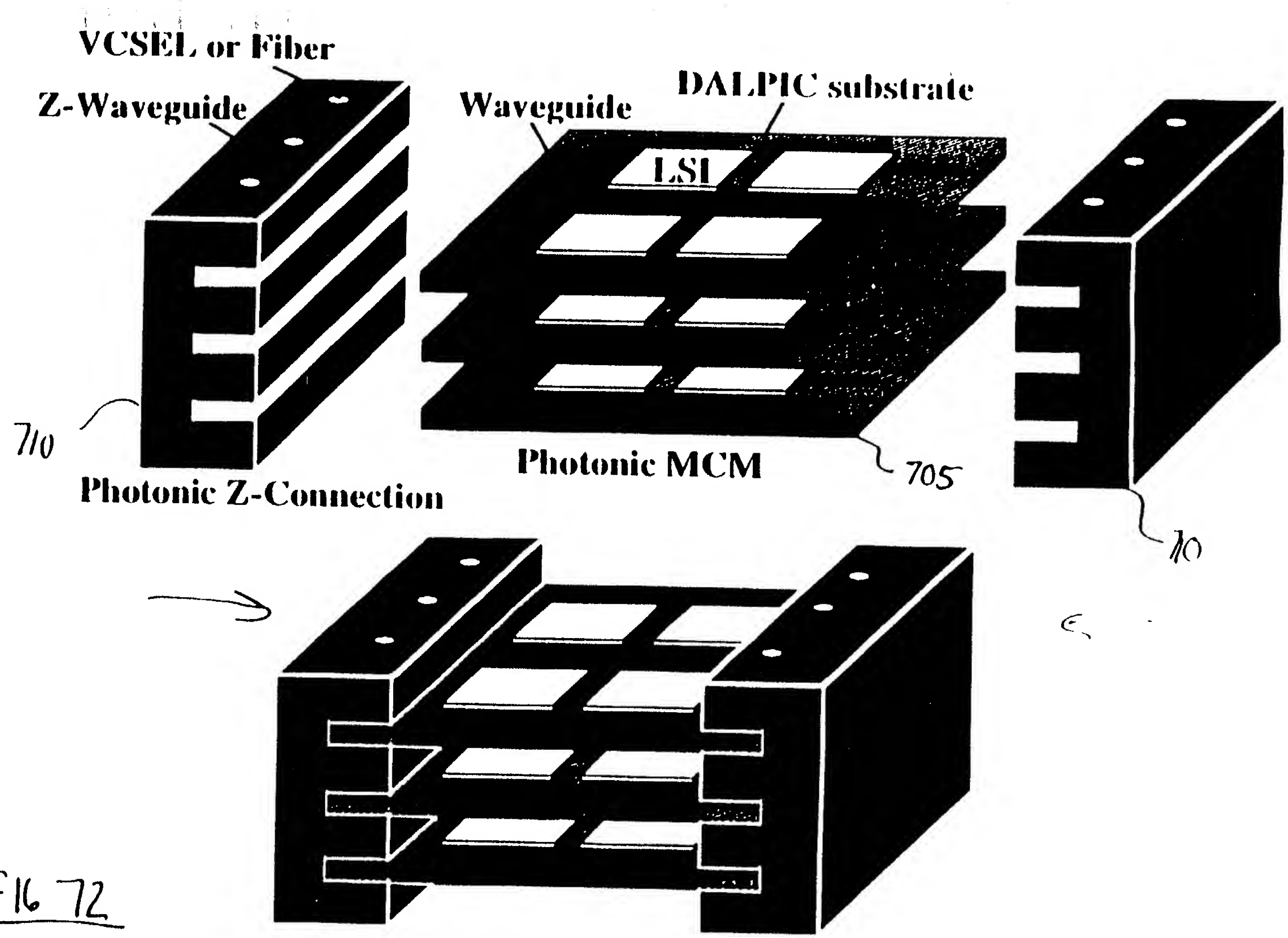
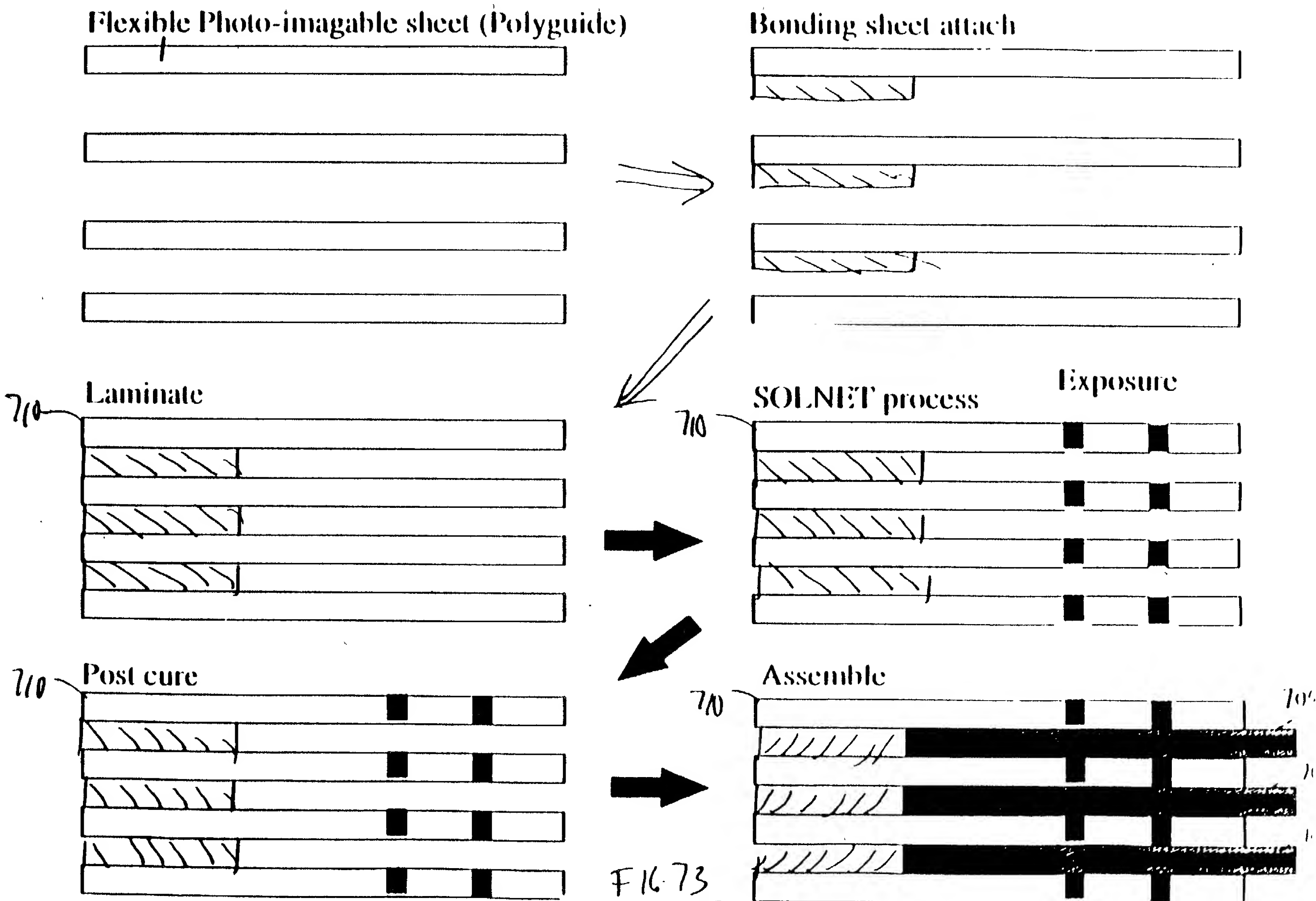

Vertical optical interconnects
Vertical optical interconnects
Z-WG/Lens
320b
Metal
320a
350
LSI
IP
LE3
LE2
LE1
LE3
LE2
LE1
LE3
LE2
Optical Z-Connection
Optical Backplane

FIG. 7



VCSEL or Fiber
Z-Waveguide
Waveguide
DALPIC substrate
LSI
710
Photonic Z-Connection
Photonic MCM
705
710

FIG 72



Flexible Photo-imagable sheet (Polyguide)
Bonding sheet attach
Laminate
710
SOLNET process
Exposure
710
Post cure
710
Assemble
710

FIG. 73

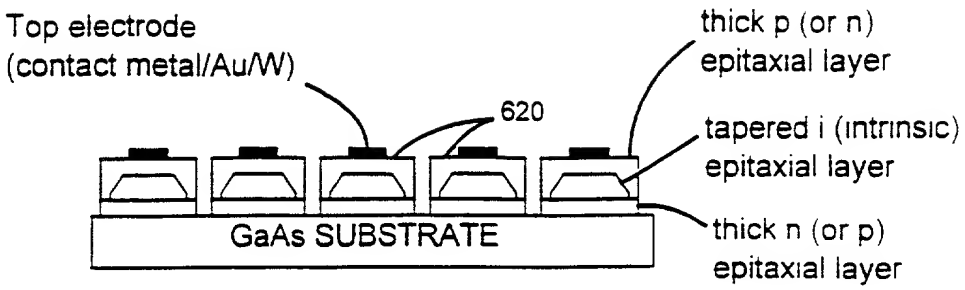


FIG._74 (Epitaxial growth and patterning)

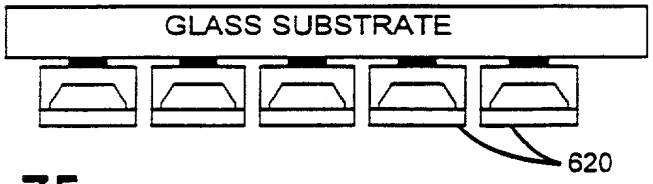


FIG._75 (Epitaxial liftoff)

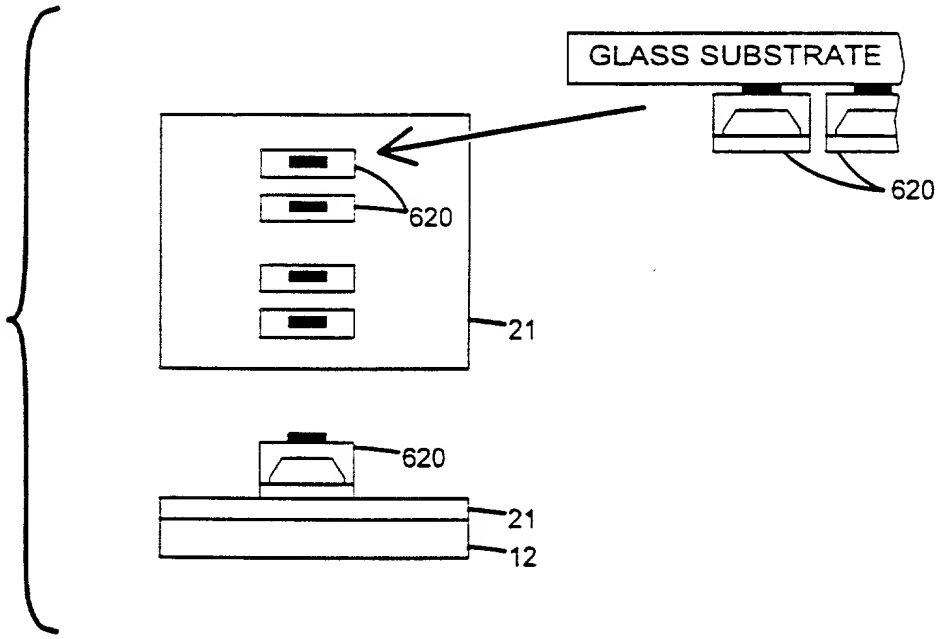
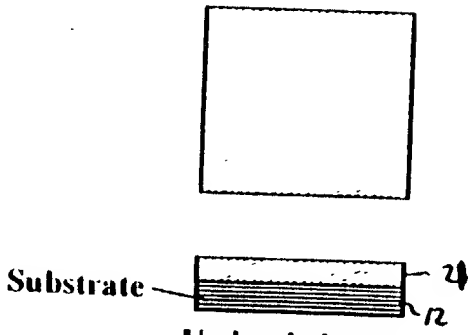
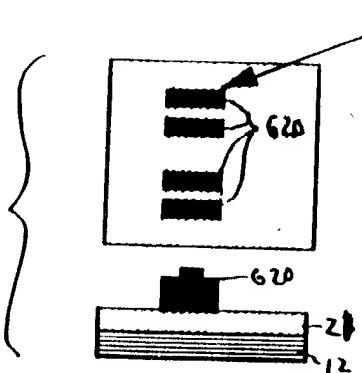


FIG._76 (Transfer)

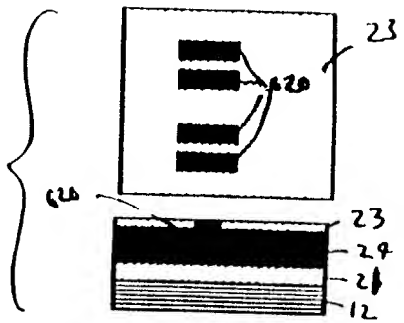


Underclad coat



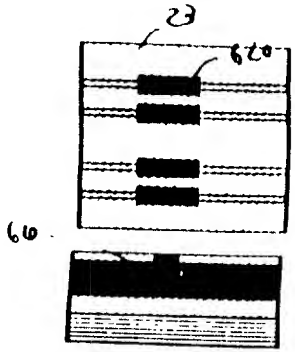
Thin-film device attatch

F16.76



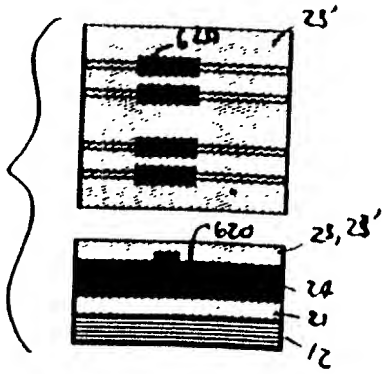
Core coat/Clad coat /CMP

F16.77



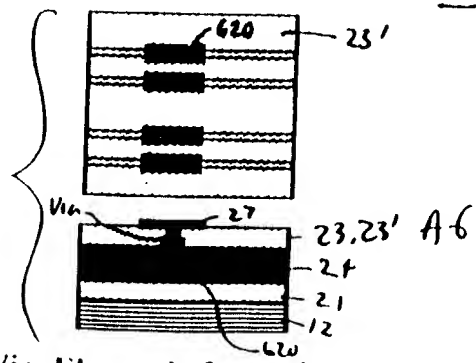
Core patterning

F16. 78



Clad coat

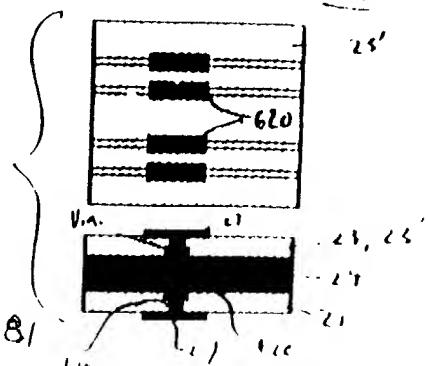
Fig. A6 F16 79



Via, Electrode formation

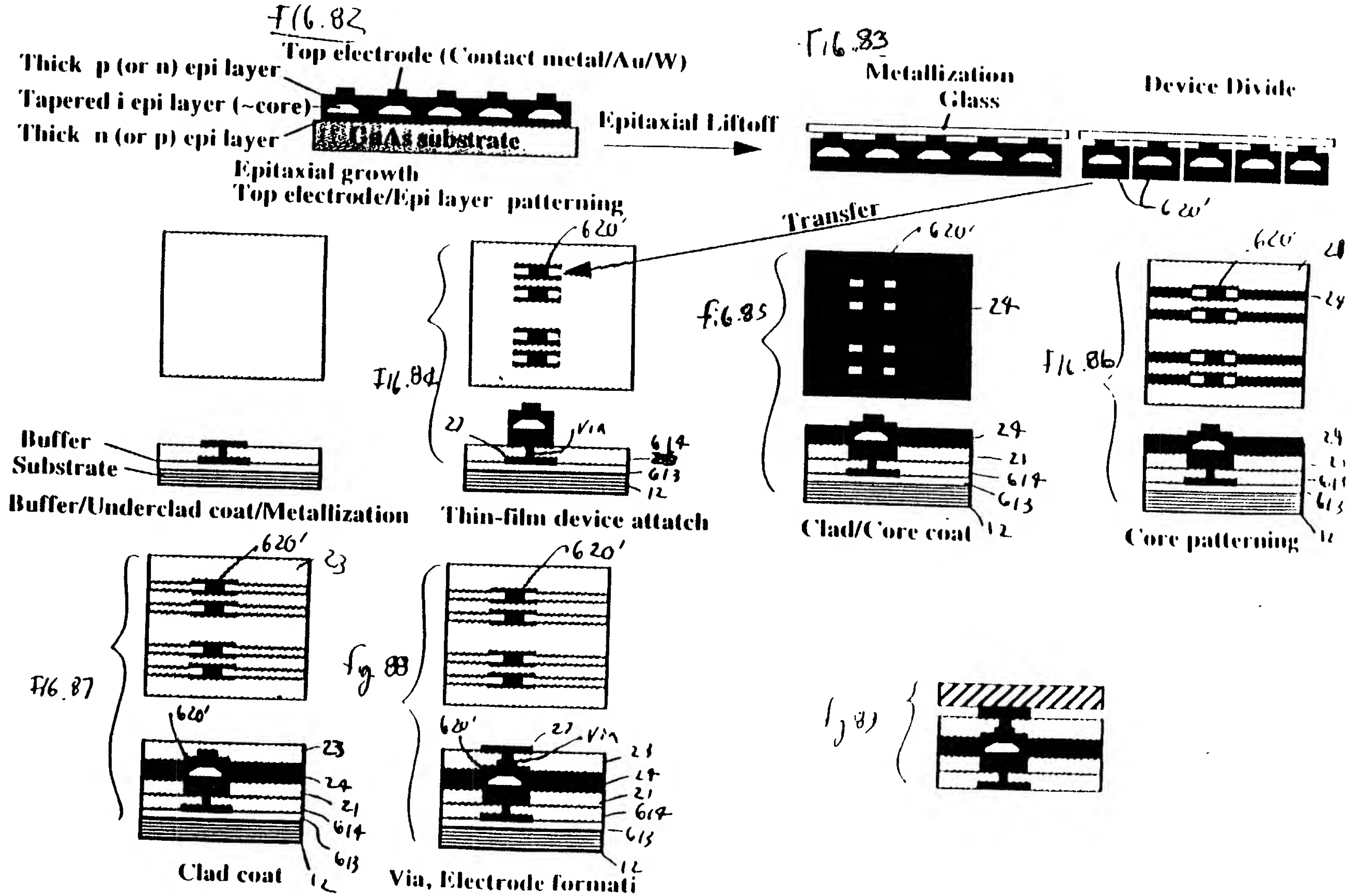
F19 80.

A6



F16. 81

Substrate removal/Back side metallization


Top electrode (Contact metal/Au/W)
Thick p (or n) epi layer
Tapered i epi layer (~core)
Thick n (or p) epi layer
GaAs substrate
Epitaxial growth
Top electrode/Epi layer patterning
Epitaxial Liftoff
Metallization
Glass
Device Divide
Transfer
Buffer
Substrate
Buffer/Underclad coat/Metallization
Thin-film device attatch
Clad/Core coat
Core patterning
Clad coat
Via, Electrode formati

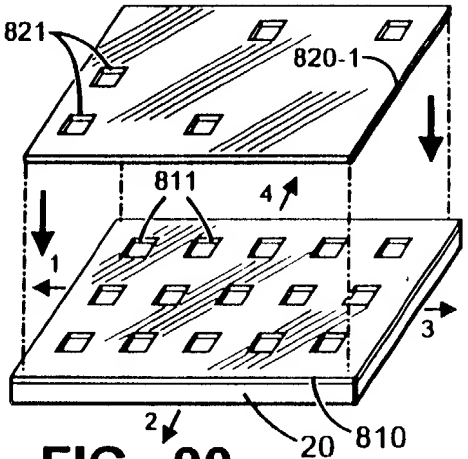


FIG._90

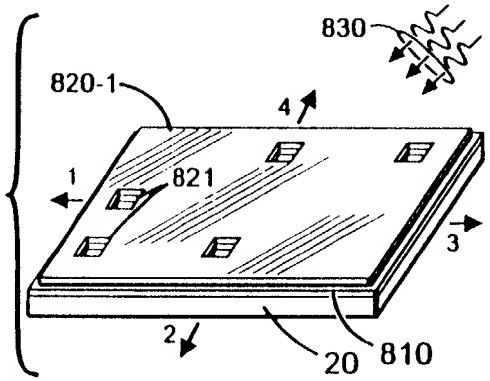


FIG._91

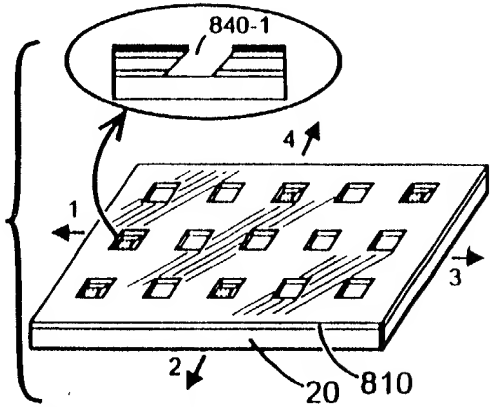


FIG._92

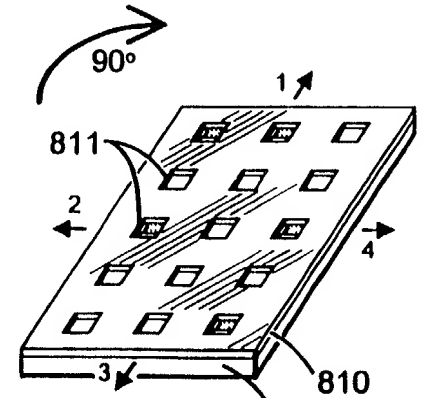


FIG._93

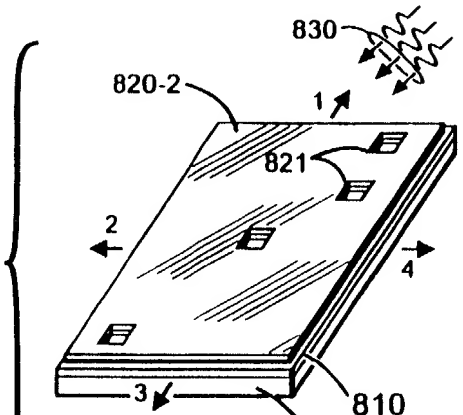


FIG._94

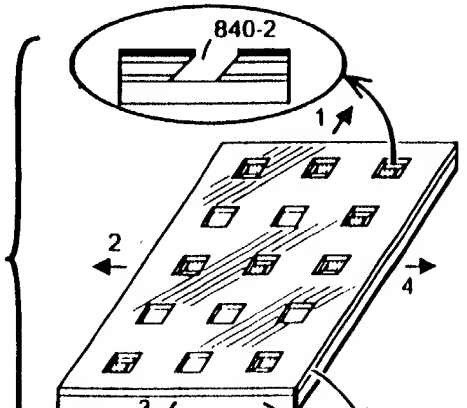


FIG._95

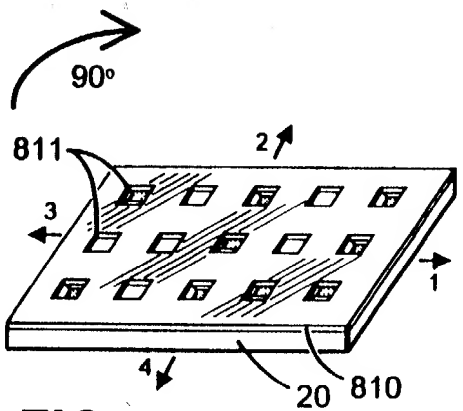


FIG._96

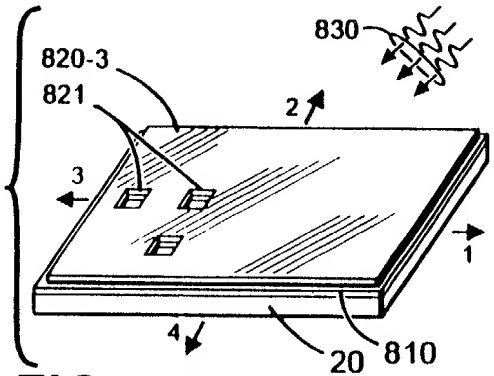


FIG._97

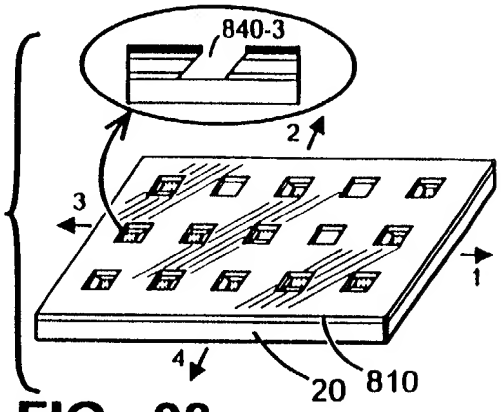


FIG._98

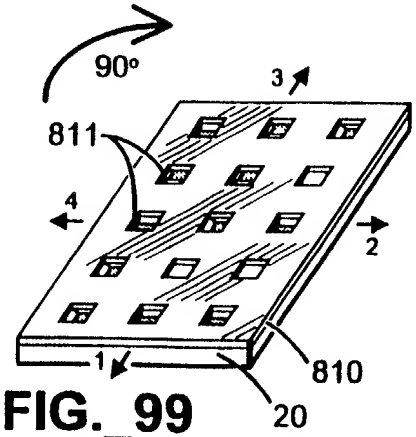


FIG._99

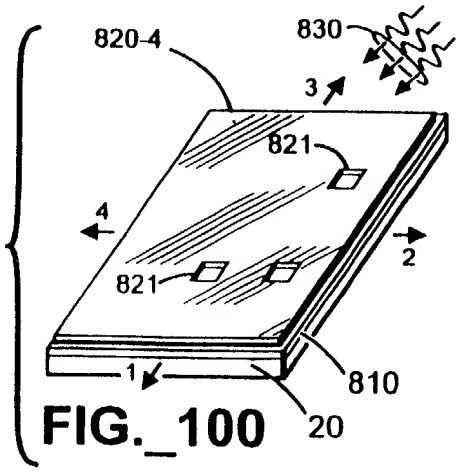


FIG._100

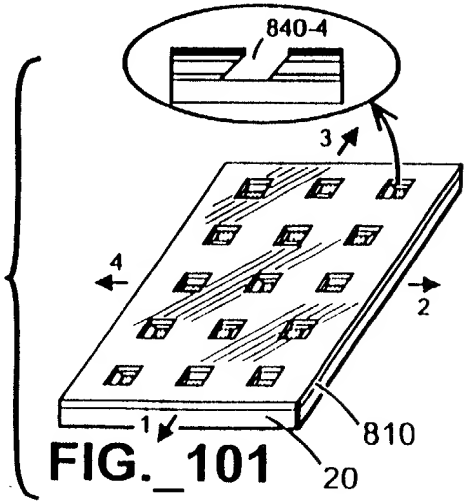


FIG._101

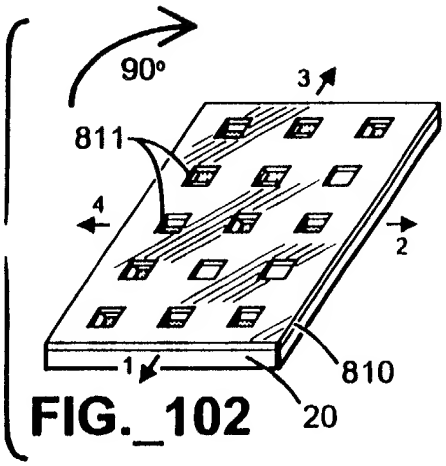


FIG._102

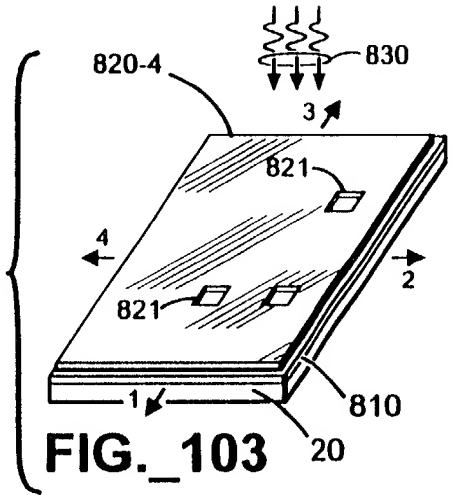


FIG._103

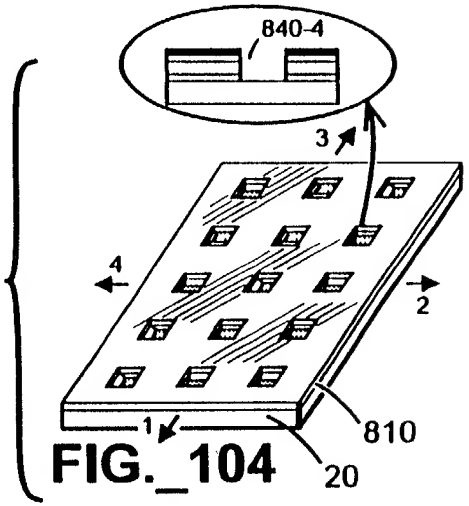


FIG._104

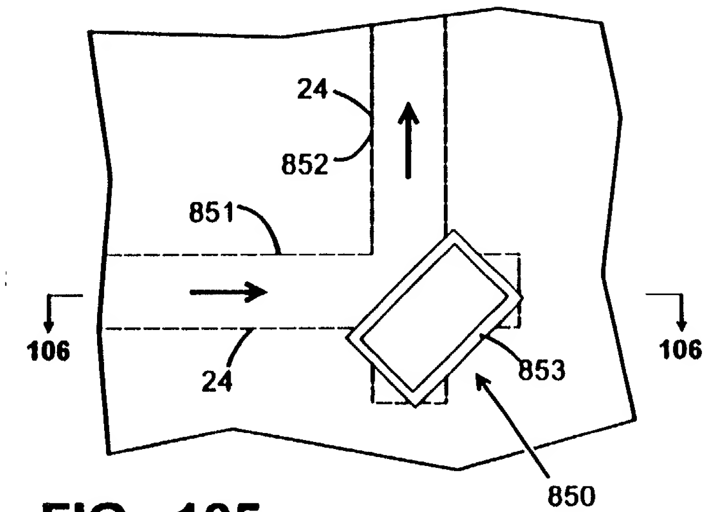


FIG._105

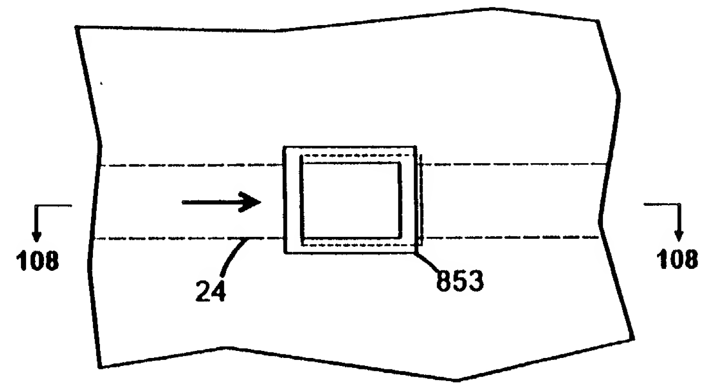


FIG._107

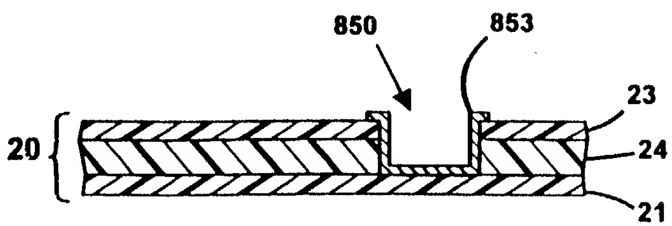


FIG._106

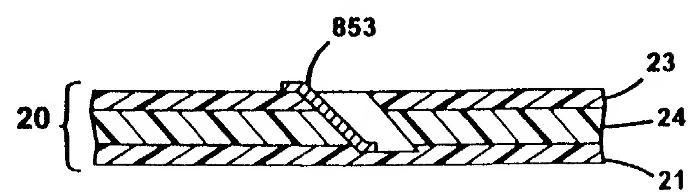
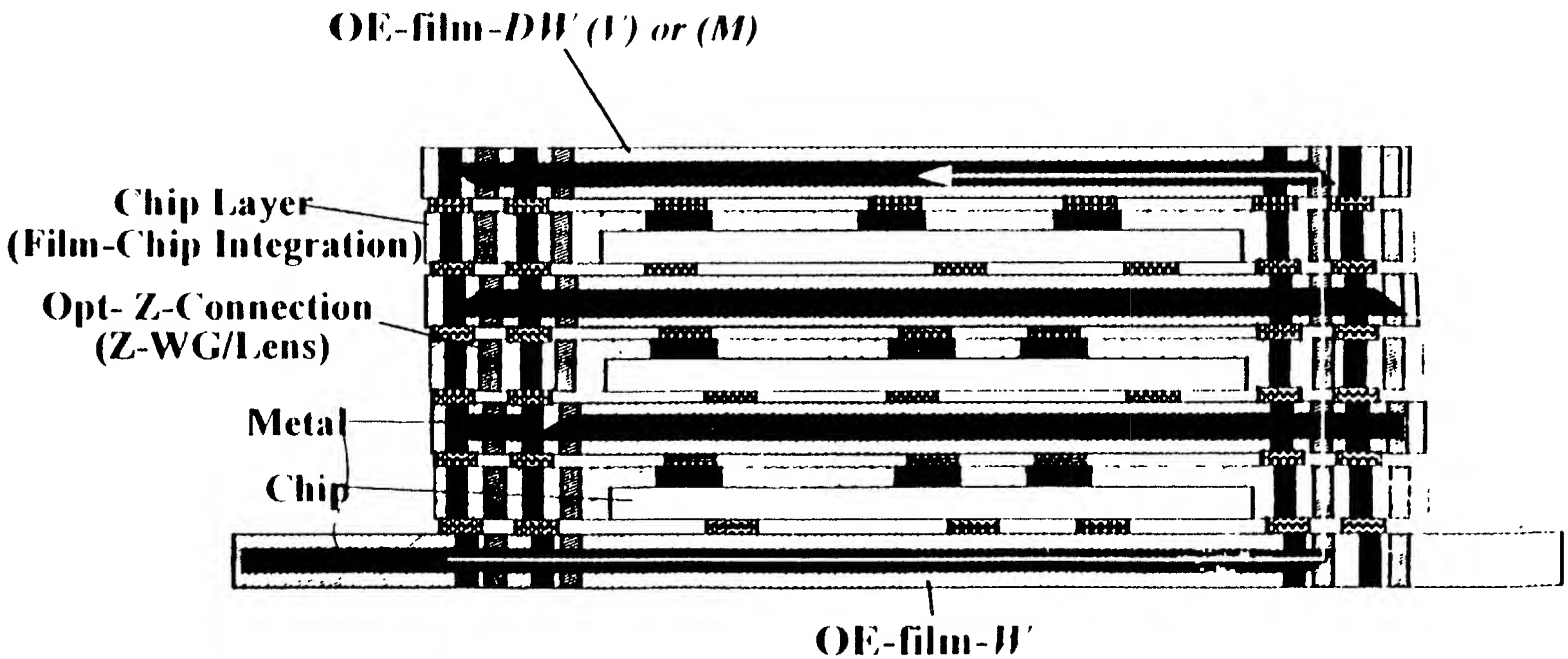


FIG._108

FUJITSU Computer Packaging Technologies, Inc. **FCPT**

GS CX/CXX OE Solution --- OE-3D-Stack



A 22

FIG. 109

<u>*2/23/99-added 7*</u>

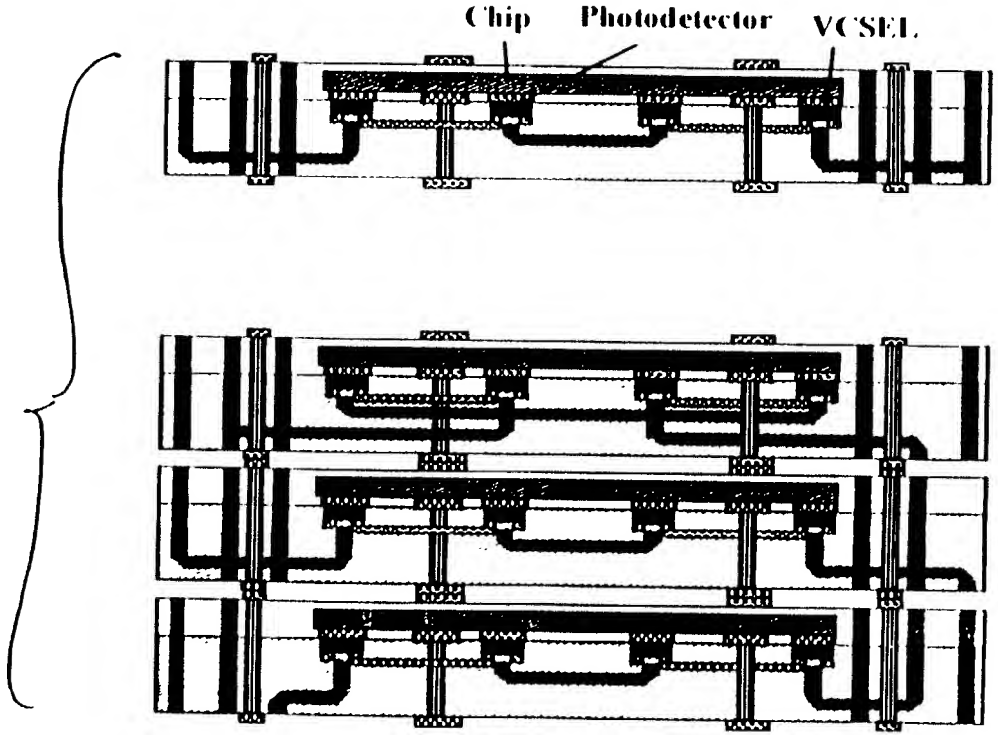


FIG. 11O

A23

(2/23/99) AA1 Detail picture Example for 3D-stack'

(New version of the AA1 of 2/5/99)

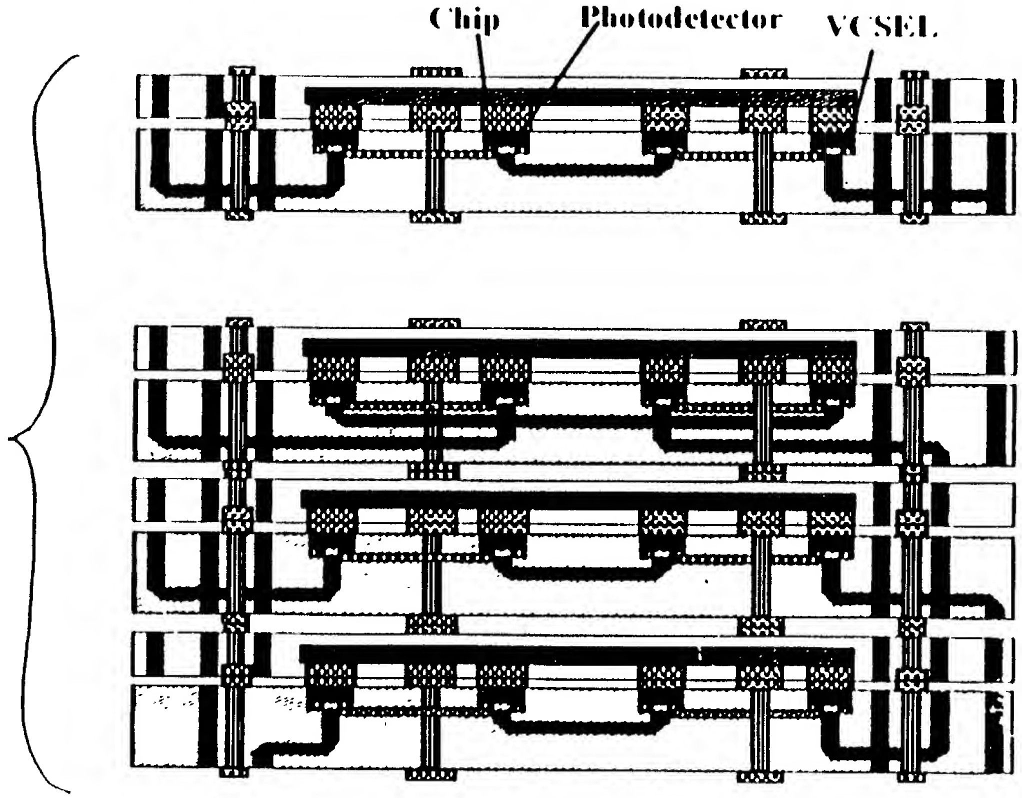


FIG. 11i

A24

(2/23/99) AA2 Detail picture Example for 3D-stack'

(New version of the AA2 of 2/5/99)

Film/Z-Connection Application to OE-Substrate

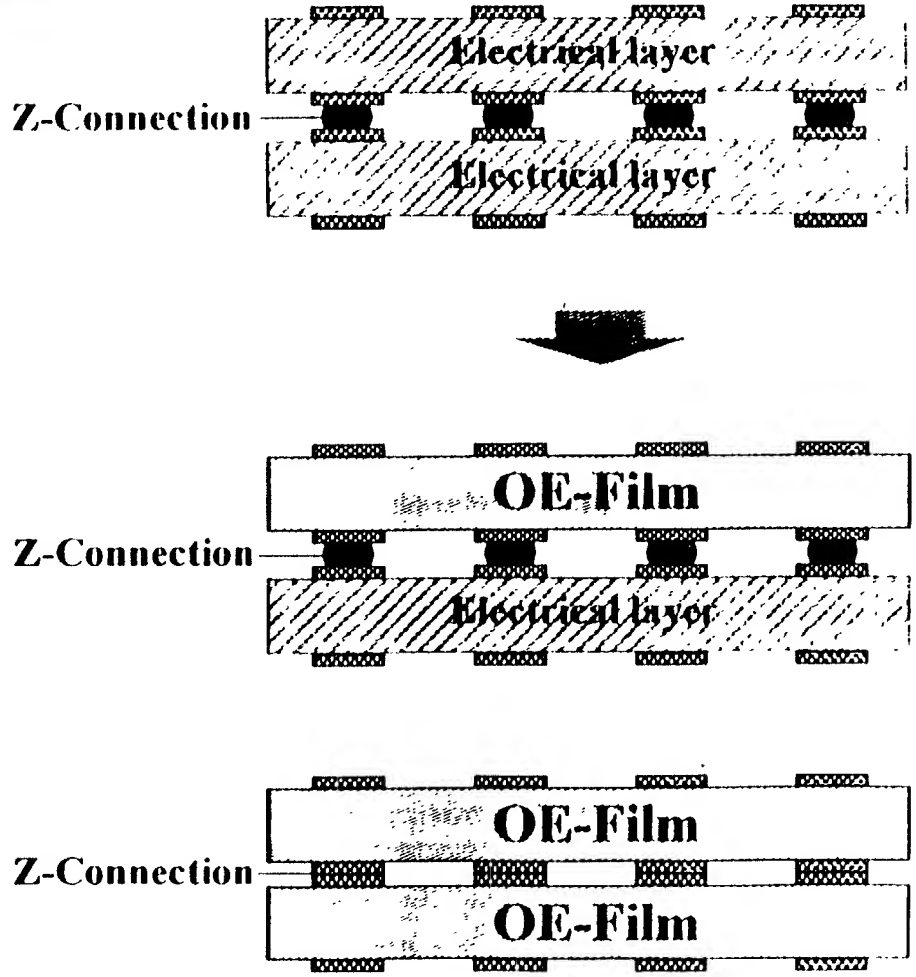


FIG. 11 2

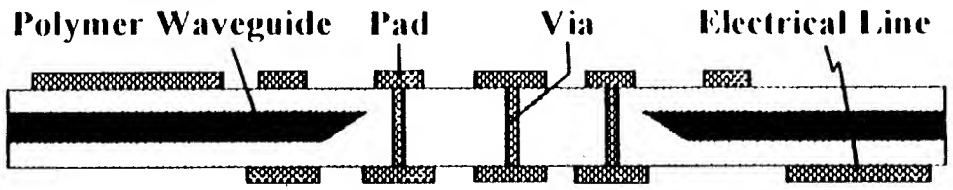
A7

2/23/99-added 1

FUJITSU Computer Packaging Technologies, Inc. FCPT

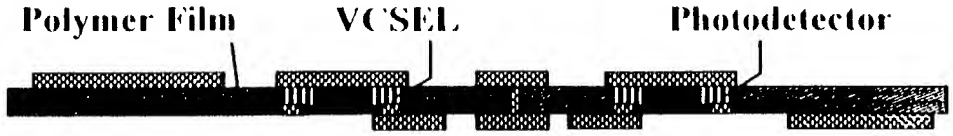
OE-Films

OE-film-*W*



F16.113

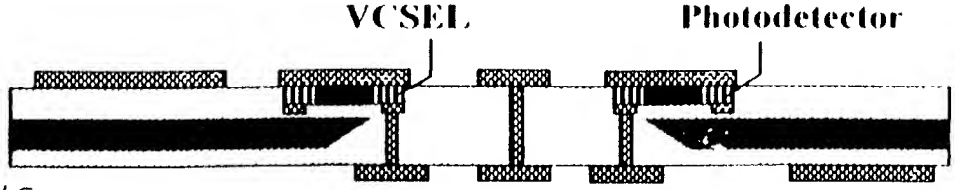
OE-film-*D*



F16.114

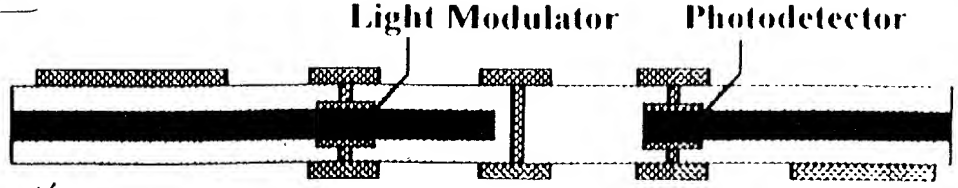
A8

OE-film-*DW(V)*



F16.115

OE-film-*DW(M)*



2/17/99-added 2

F16.116

FOLM

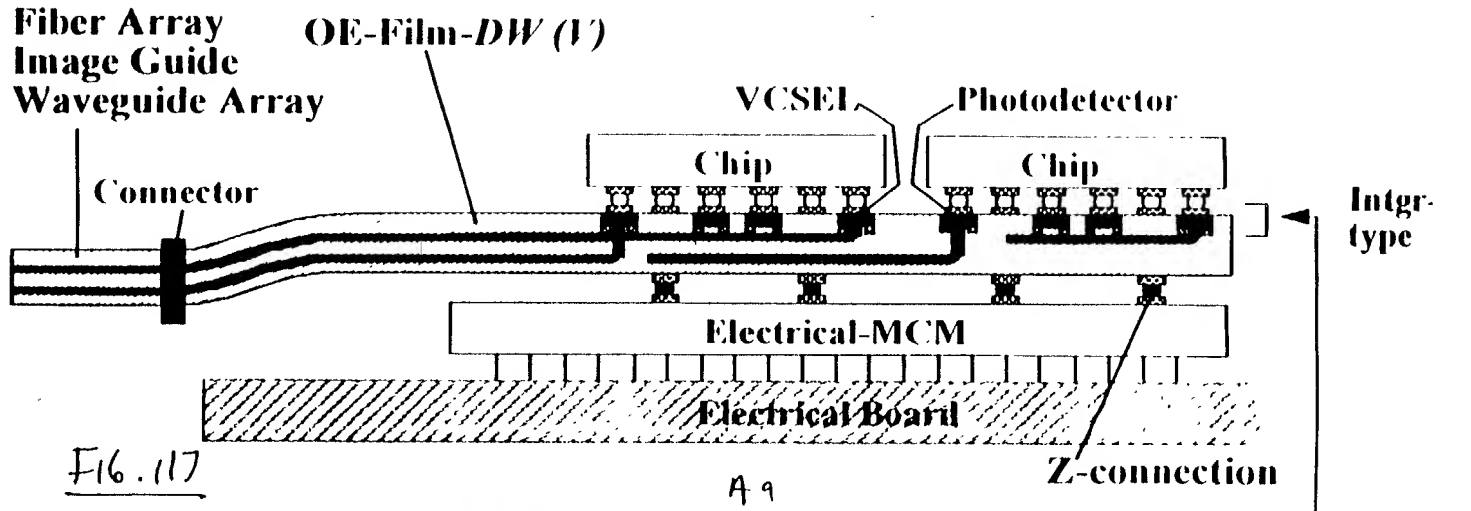
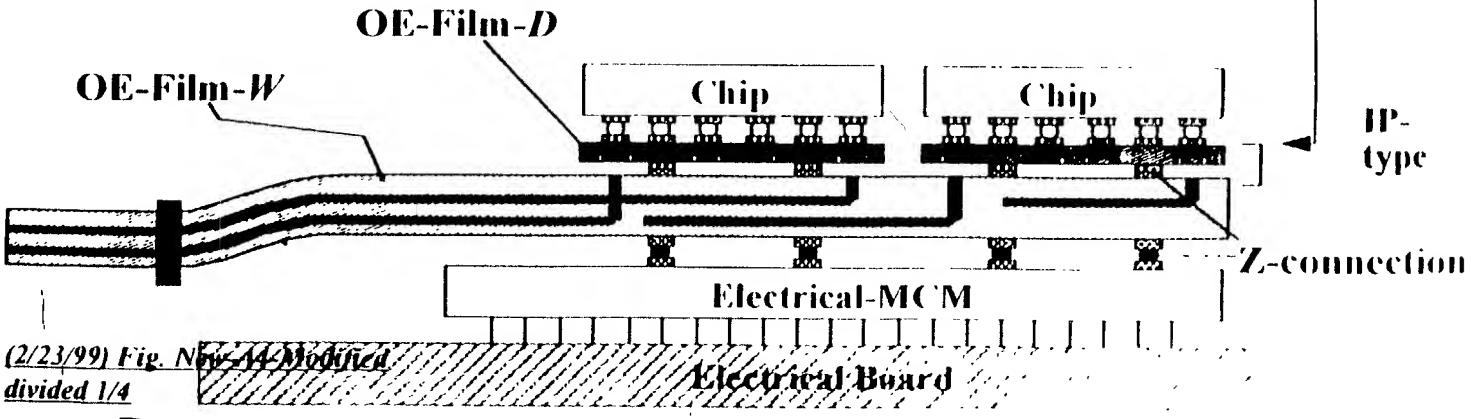


FIG. 117

A9



(2/23/99) Fig. News-14-Modified divided 1/4

FIG. 118

FOLM

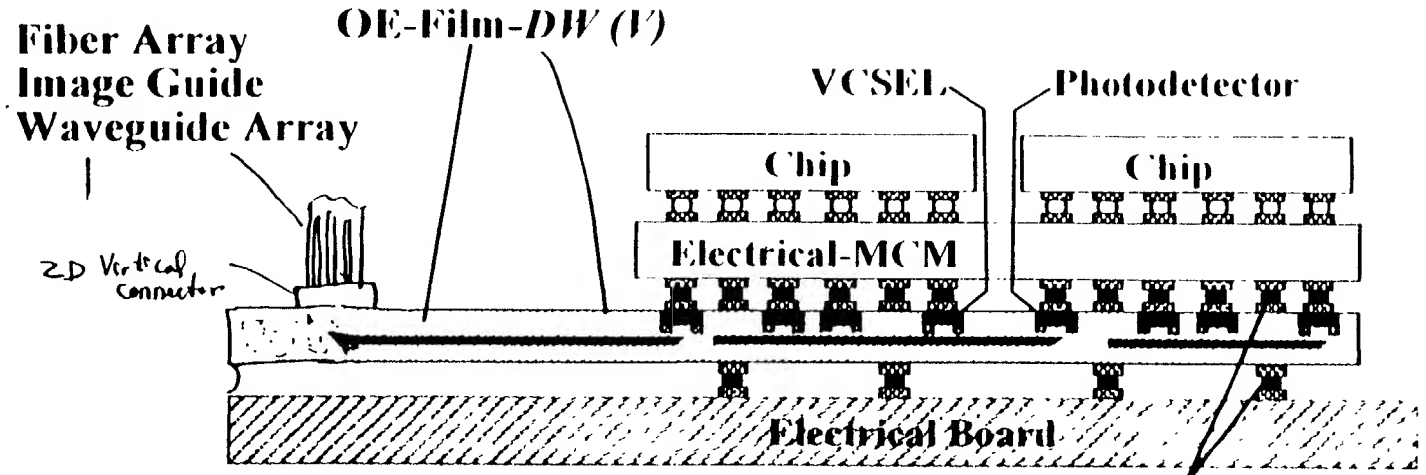


Fig. 11a

A10

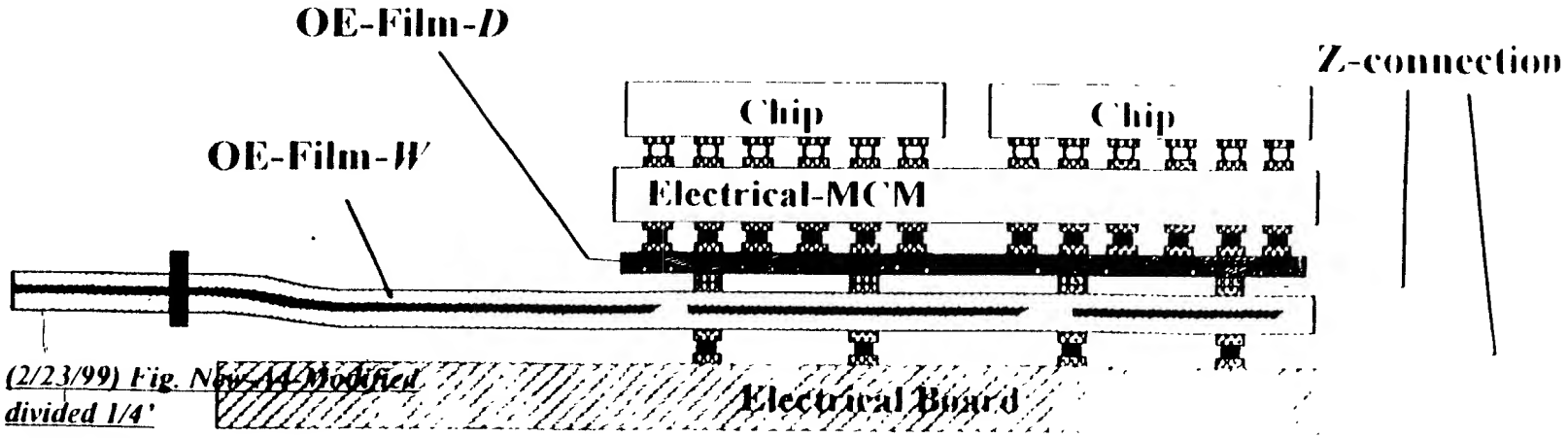
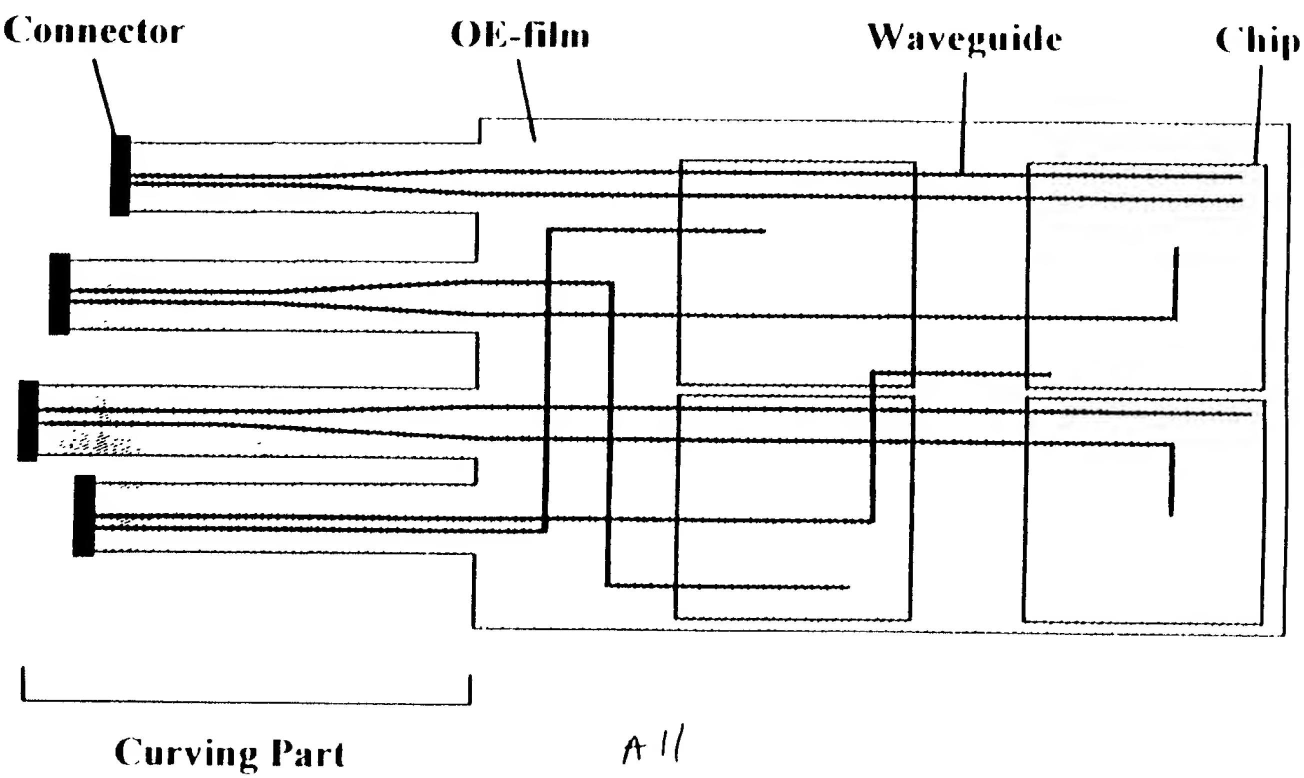


Fig. 11b

FUJITSU Computer Packaging Technologies, Inc. FCPT

FOLM with Optical Path Length Controller, Connector Buffer

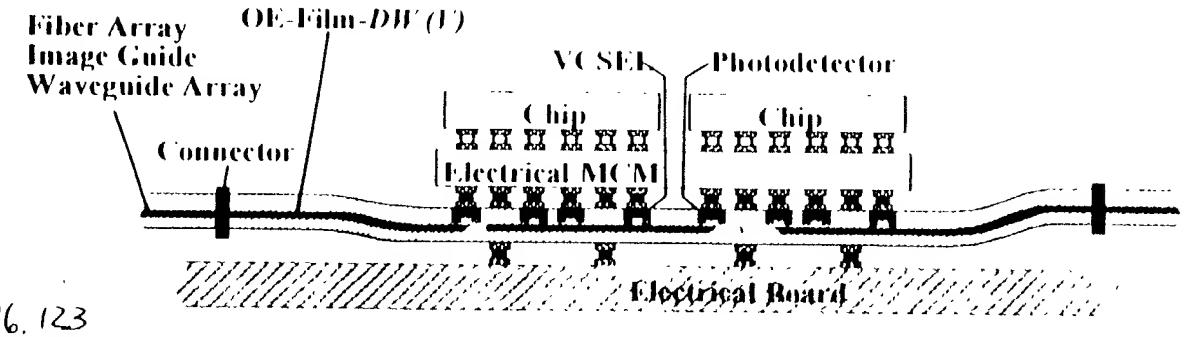


A 11

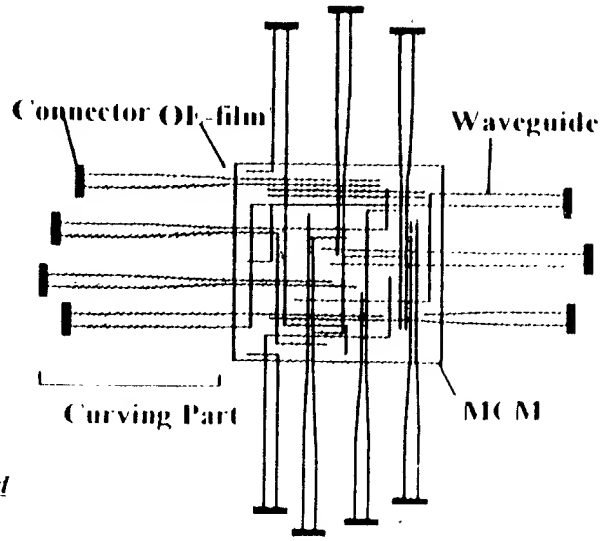
FIG. 121

(2/17/99) Fig. New-A4-Modified divided 2/4

FOLM with Optical Path Length Controller, Connector Buffer



F16. 123

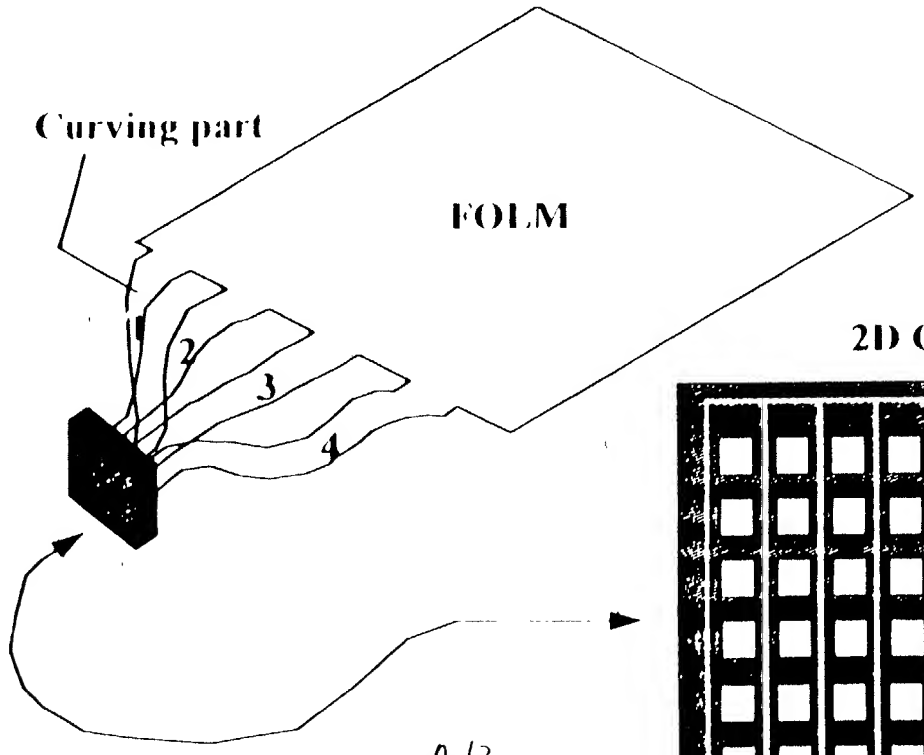


F16. 122

(2/23/99) Fig. New-A4-Modified divided 2/4'

FUJITSU Computer Packaging Technologies, Inc. FCPT

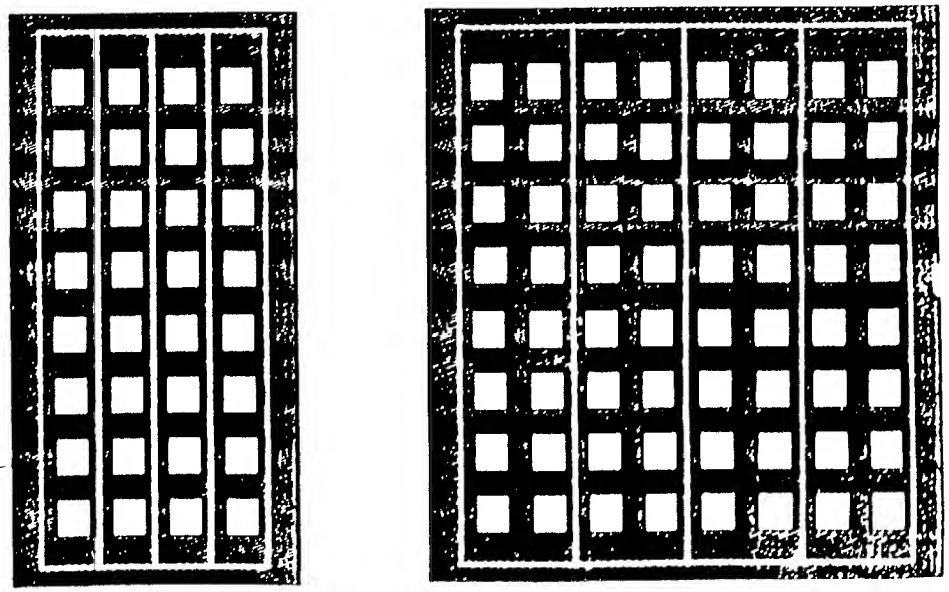
FOLM with 2D Waveguide Connector



A 13

F16. 12A

2D Connector cross-section



(for Single-layer waveguide) (for 2 layer waveguide)

(2/23/99) Fig. New-14-Modified divided 3/4'

FOLM: High-Speed Option

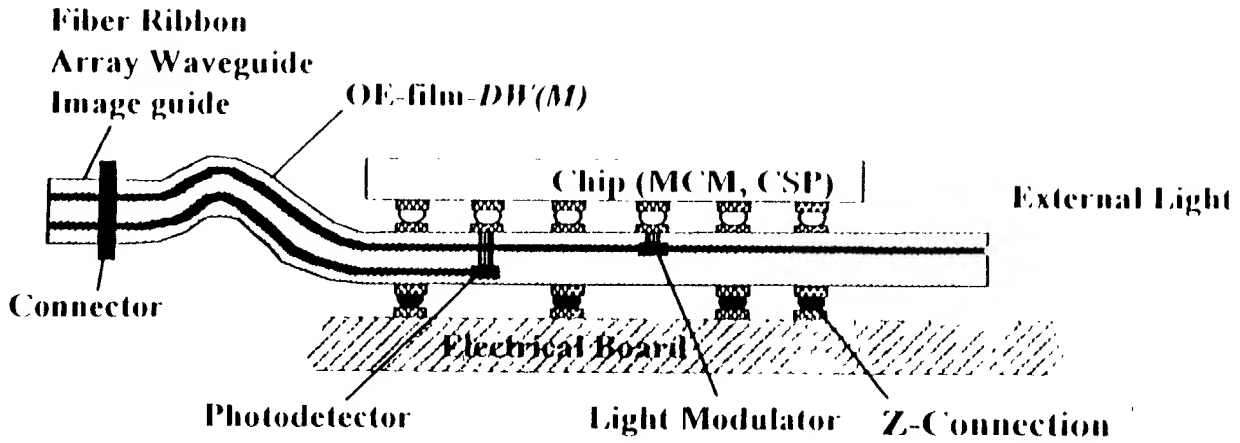


Fig 125

A 14

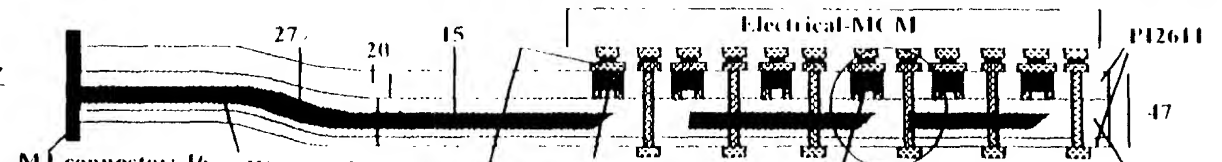
(2/17/99) Fig New-A4-Modified divided 4/4

FUJITSU Computer Packaging Technologies, Inc. **FCPT**

FOLM Structure Example (Overall)

Through put: 1.5 pbs x 196 ch   Assume SSN MCM Size is 5 cm x 5 cm   Unit: um

FIG. 126



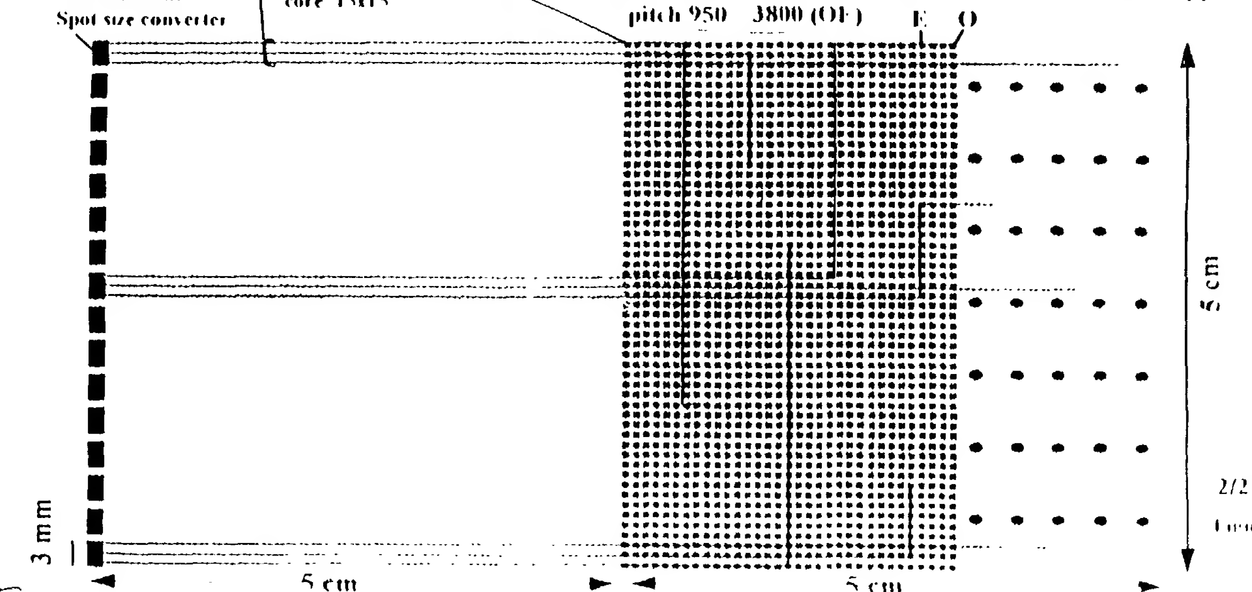
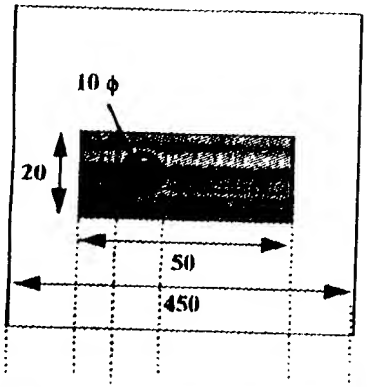


FIG. 127

FUJITSU Computer Packaging Technologies, Inc. FCPT

FOLM Structure Example (VCSEL part)

FIG. 12A



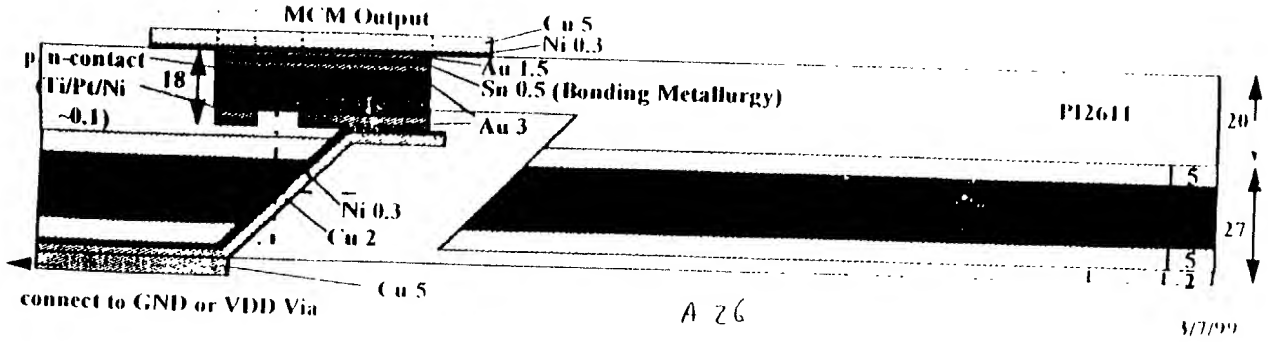


FIG. 12B

Unit : um

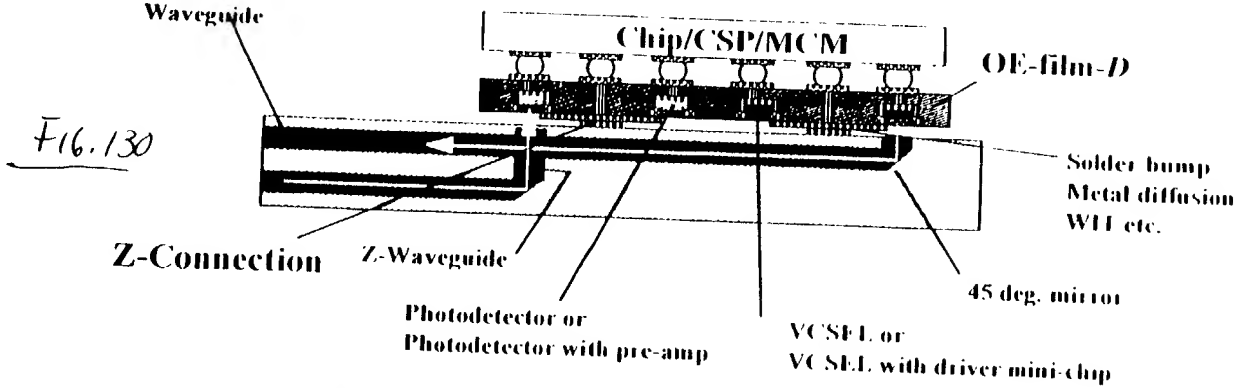
A 26

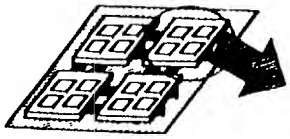
3/7/99

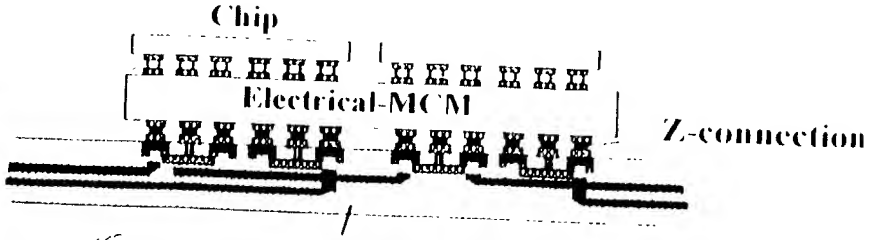
FUJITSU Computer Packaging Technologies, Inc. FCPT

OE-film: OE-IP, OE-Film-MCM

F16.130







F16.131

A15

(2/23/99) Fig. New-A1-Modified

FUJITSU Computer Packaging Technologies, Inc. FCPT

OE-film: Light Modulator Transmitters

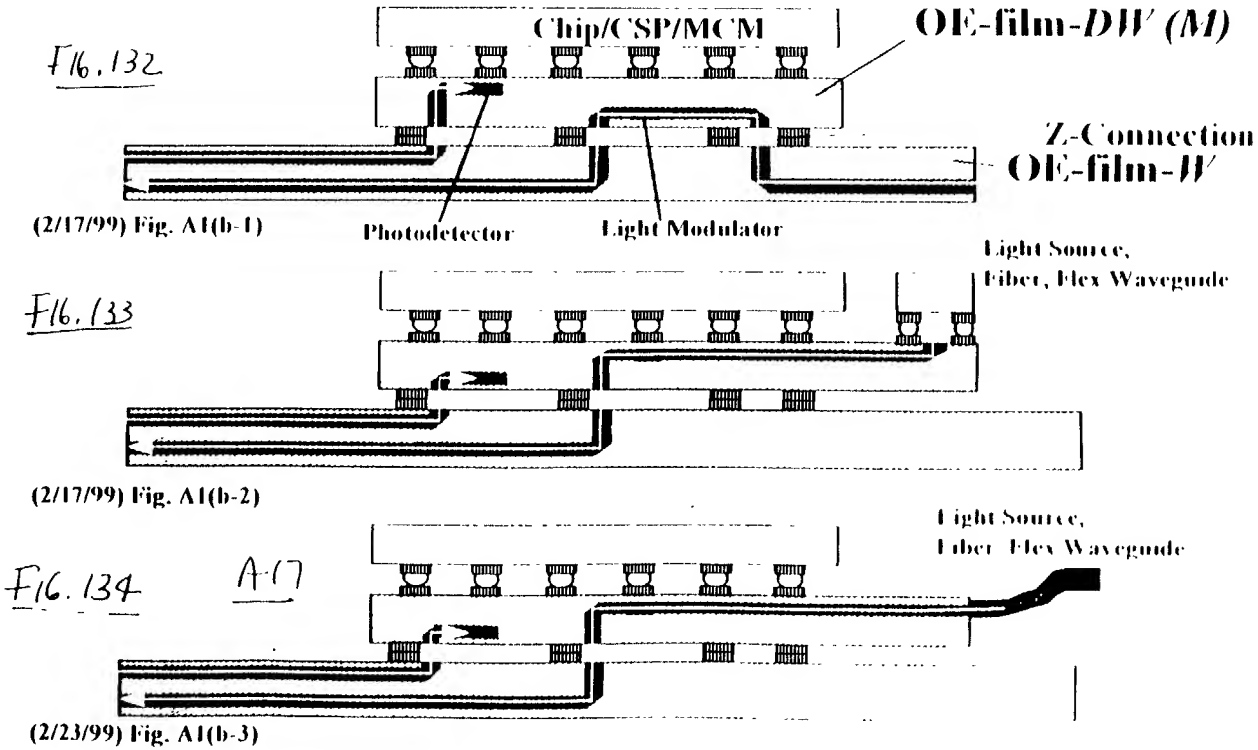


Fig. 132

(2/17/99) Fig. A1(b-1)

Fig. 133

(2/17/99) Fig. A1(b-2)

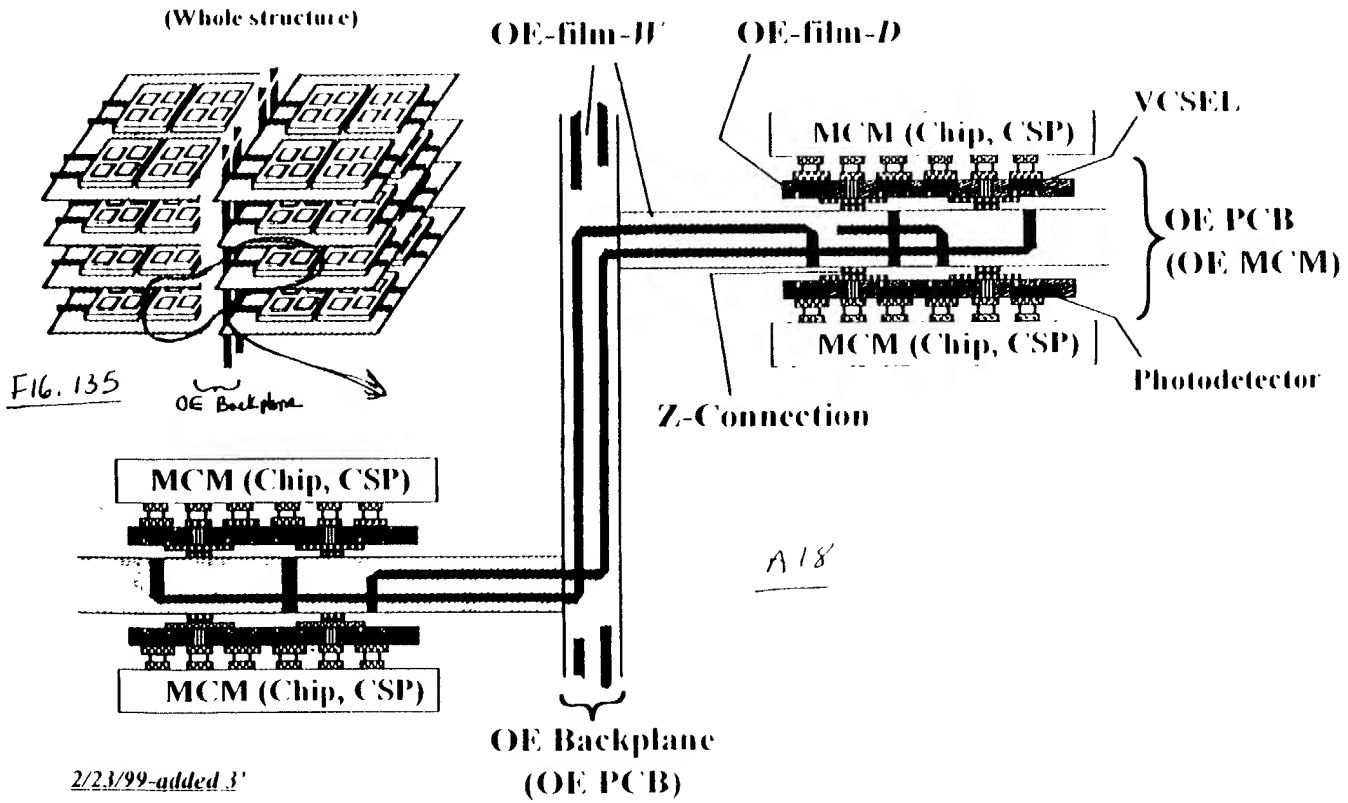
Fig. 134 A-17

(2/23/99) Fig. A1(b-3)

Examples of Light Modulators: Electro Optic (EO) Modulator, Electro Absorption (EA) Modulator

FUJITSU Computer Packaging Technologies, Inc. FCPT

OE-film: Both-Side Packaging



F16. 135

OE Backplane

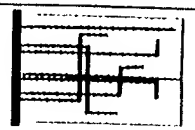
A18

2/23/99-added 3'

FUJITSU Computer Packaging Technologies, Inc.

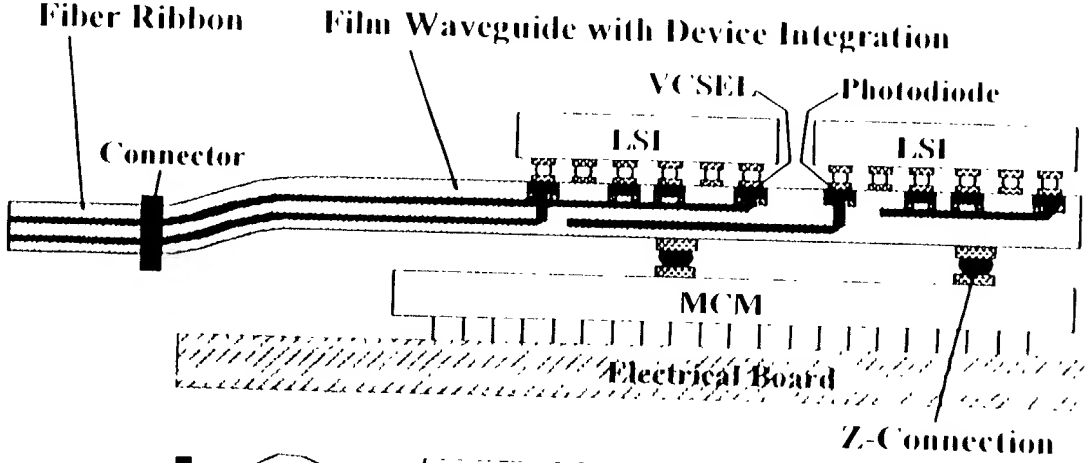
FC

Direct Jump from LSI



Can act as
Line length contr

F16.136



F16.137

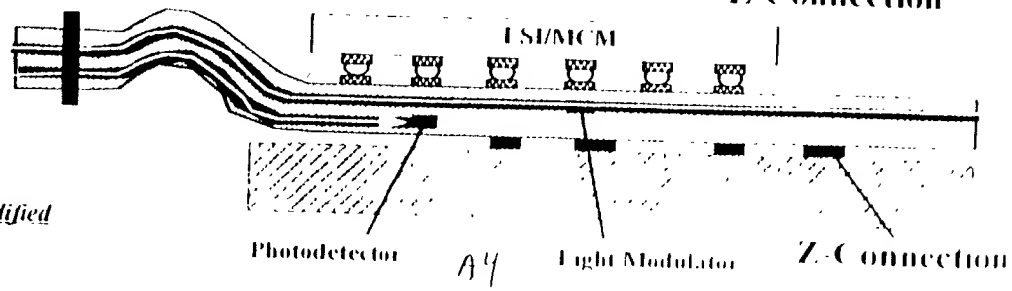
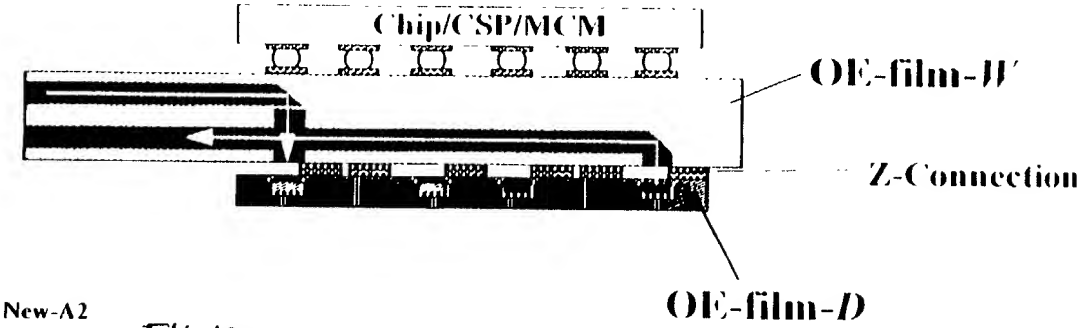


Fig. New-A4-Modified

A4

Computer Packaging Technologies, Inc. FCPT

OE IP is Placed on the Oposit Side



(2/23/99) Fig. New-A2

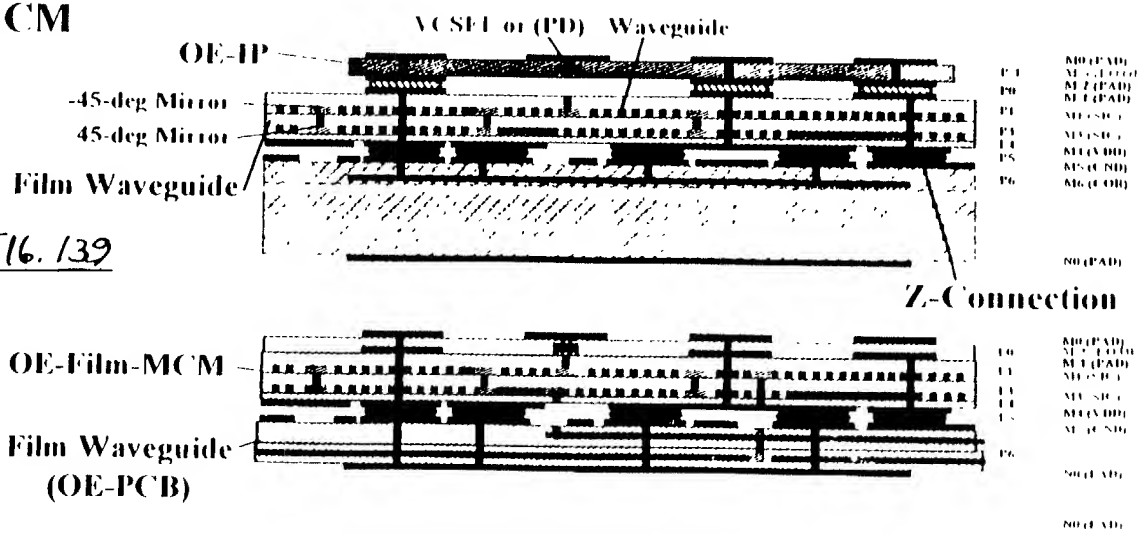
FIG. 13B

A20

OE MCM

OE-MCM

GS
MPS
PC



F16. 139

F16. 140

A5

Fig. A5-Modified

OE-film: Smart Pixel

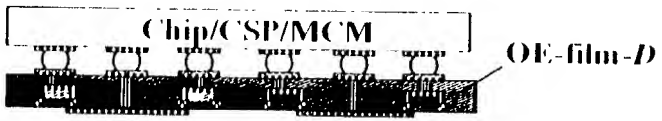


Fig 141

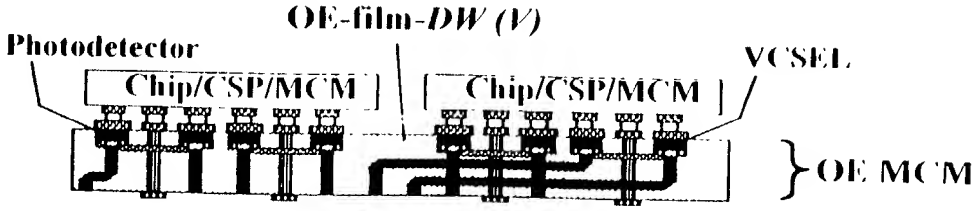


Fig. 142

A16

2/23/99-added 6'

OE-Film/OE-Film Stack --- Back-Side Connection

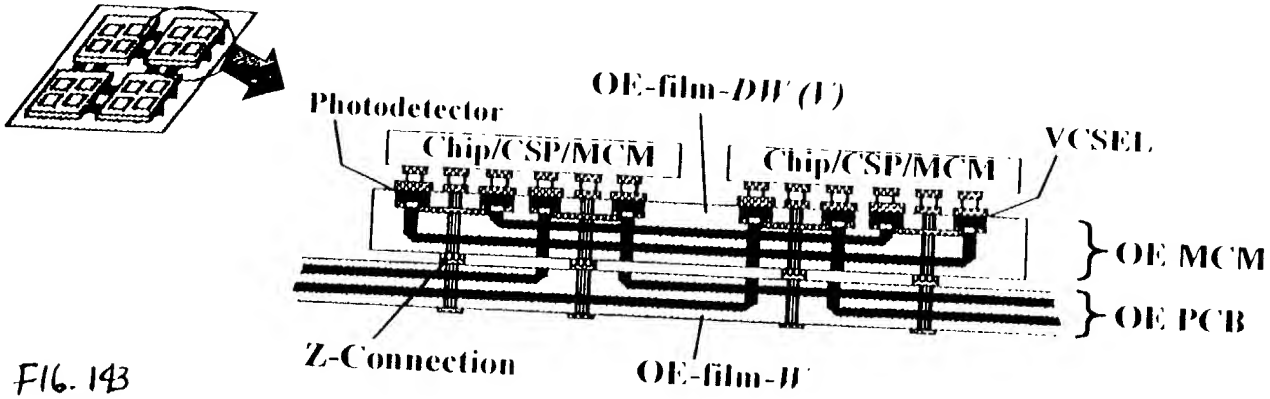
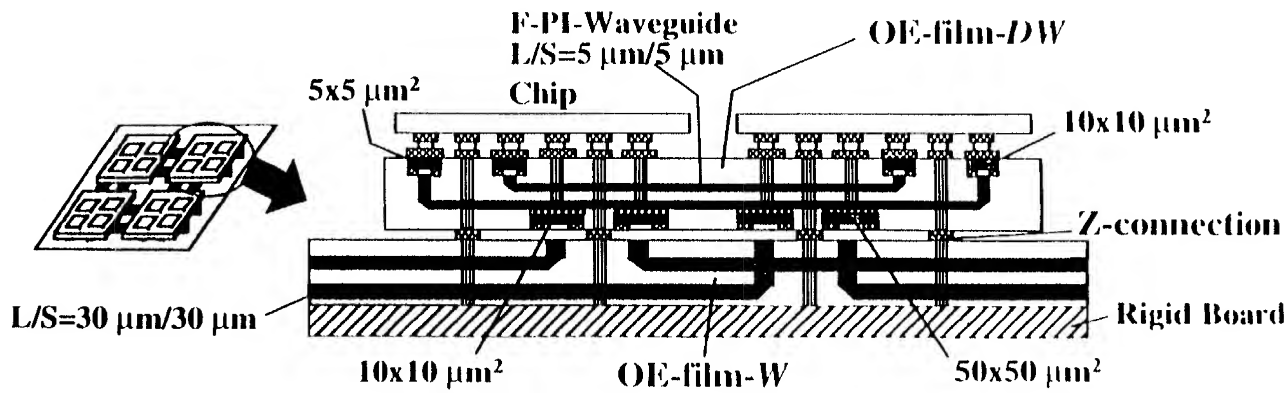


FIG. 14B

2/23/99-added 4'

FUJITSU Computer Packaging Technologies, Inc. FCPT

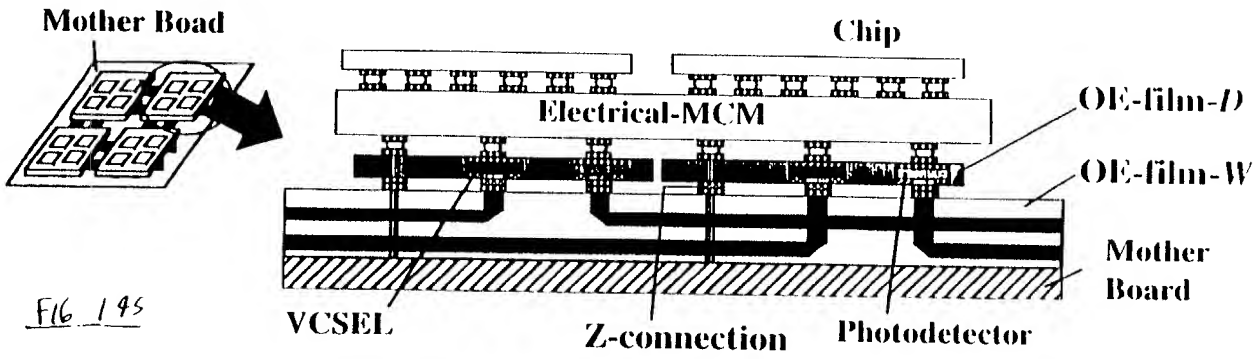
OE-Film/OE-Film Stack --- Back-Side Connection



D1

FIG 144

OE-MCM/OE-Bord Stack



F16 195

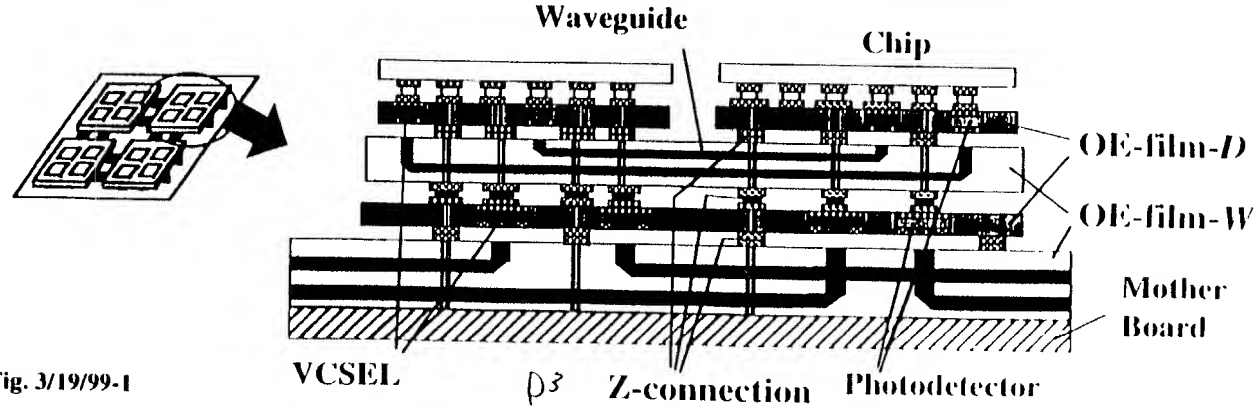


Fig. 3/19/99-1

F16 196

D3 3/18/99

Device Integration Process

(1) Pads/Lines formation

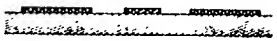


FIG. 147

(2) Placement of Thin film devices

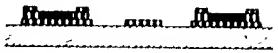


FIG. 148

(3) Polymer coat

FIG 149

(4) Planarization

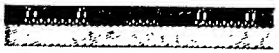


FIG 150

(5) Vias/Pads/Lines formation

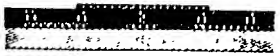


FIG 151

(6) Substrate removal

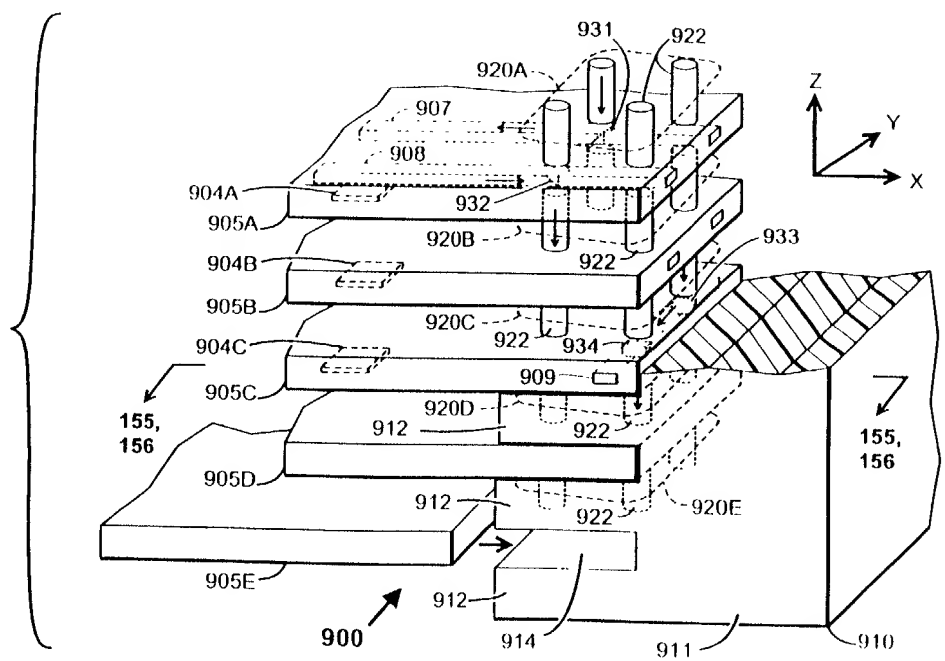
FIG. 152

OE-film-*D*

(6') Jump to the waveguide formation process

FIG. 153

OE-film *DW(1)*



931
922
920A
907
908
904A
932
905A
920B
922
904B
933
905B
920C
922
934
904C
909
905C
155,
156
920D
912
922
155,
156
905D
912
922
920E
905E
912
900
914
911
910
Z
Y
X

FIG._154

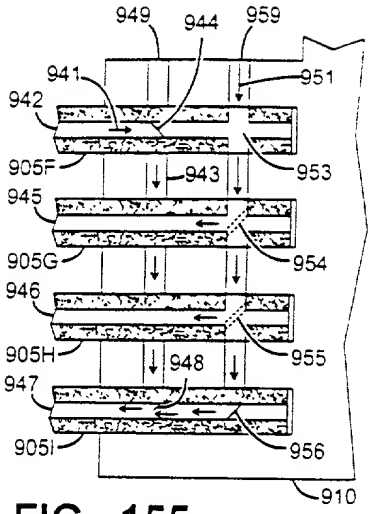


FIG._155

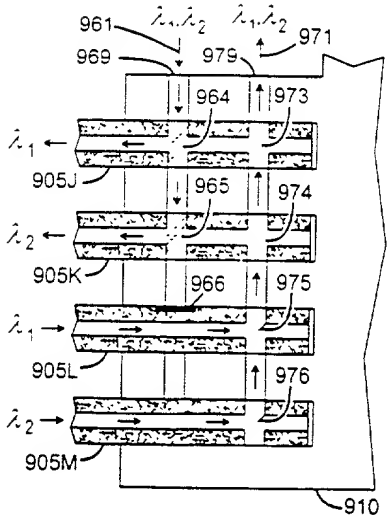


FIG._156-1

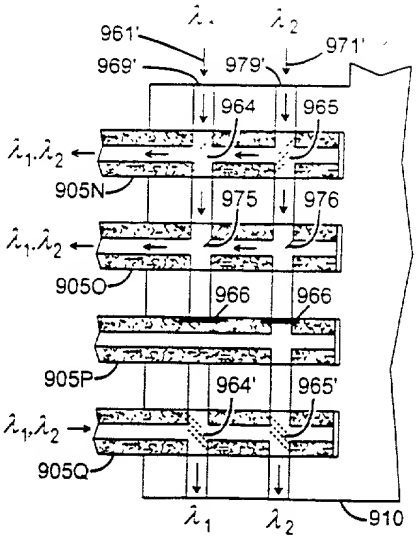


FIG._156-2

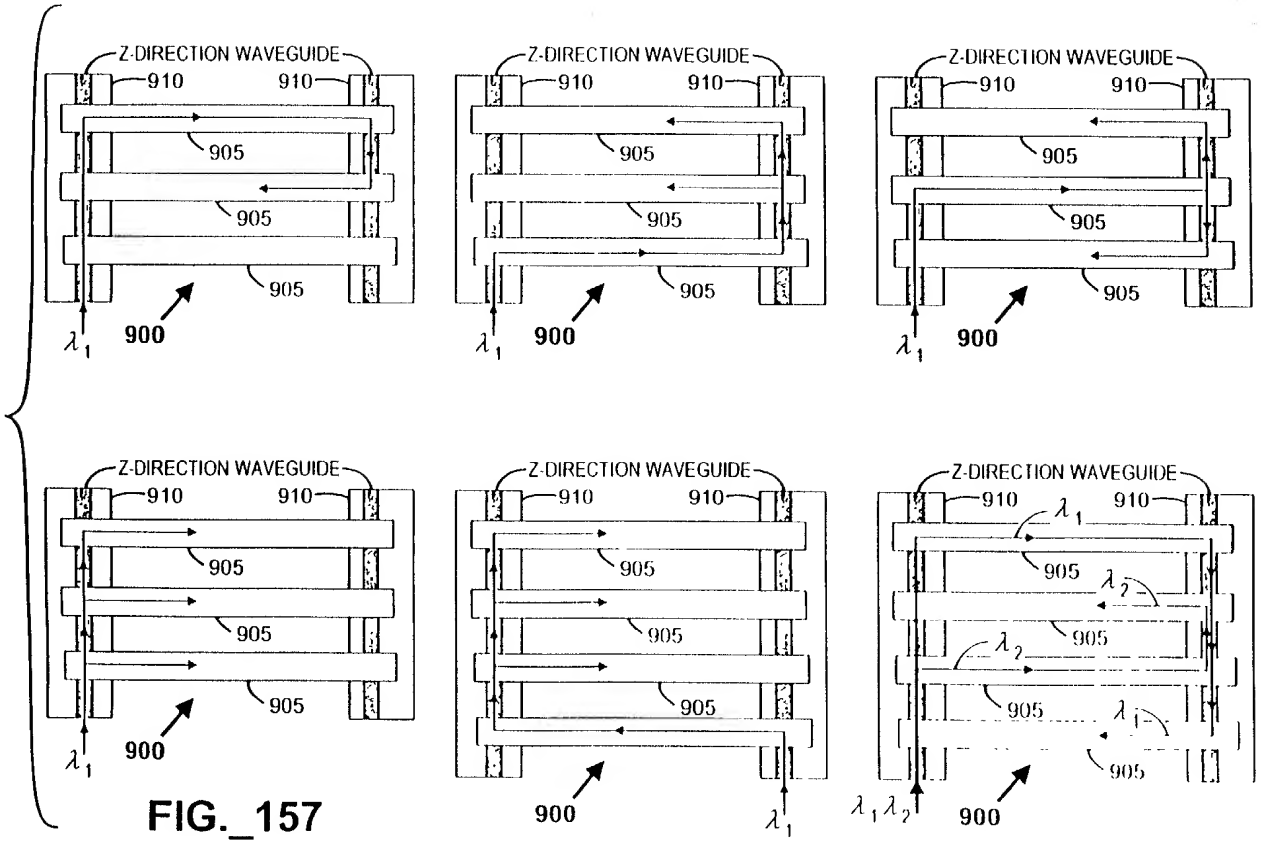

Z-DIRECTION WAVEGUIDE
910
910
905
905
905
900
λ_1
λ_2

FIG._157

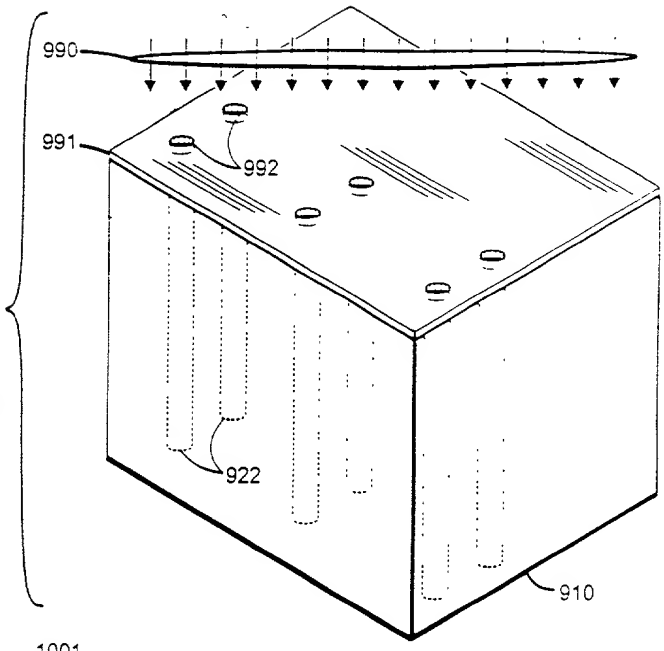


FIG._160

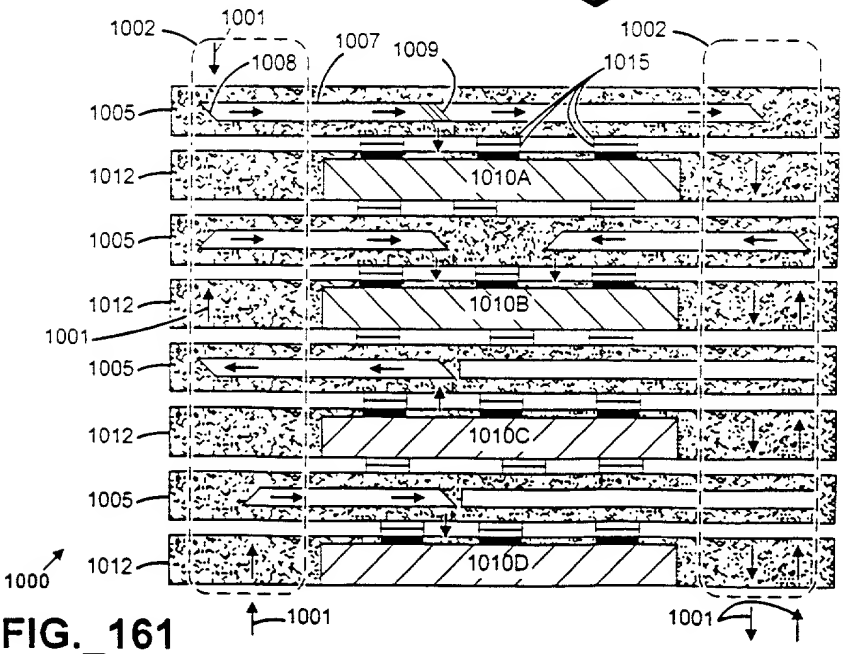


FIG._161

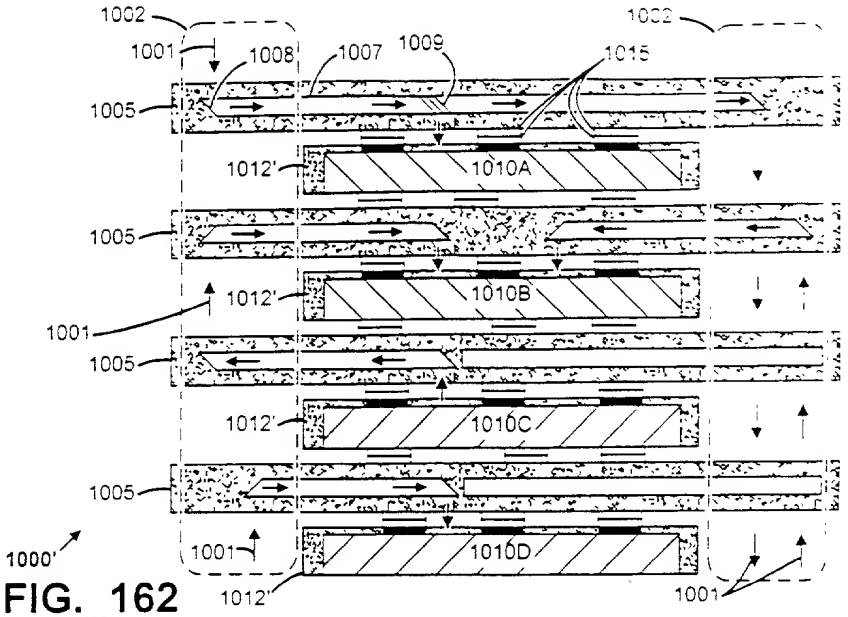


FIG._162

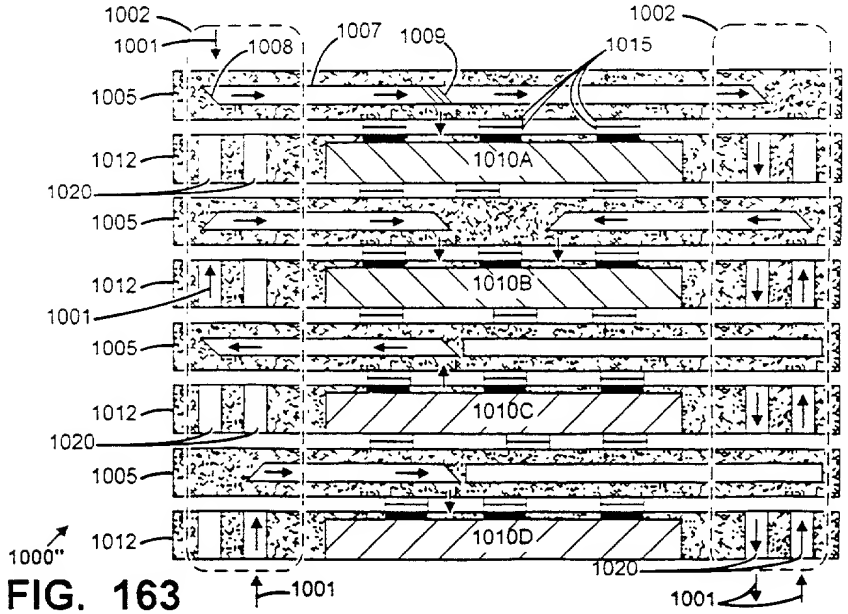


FIG._163

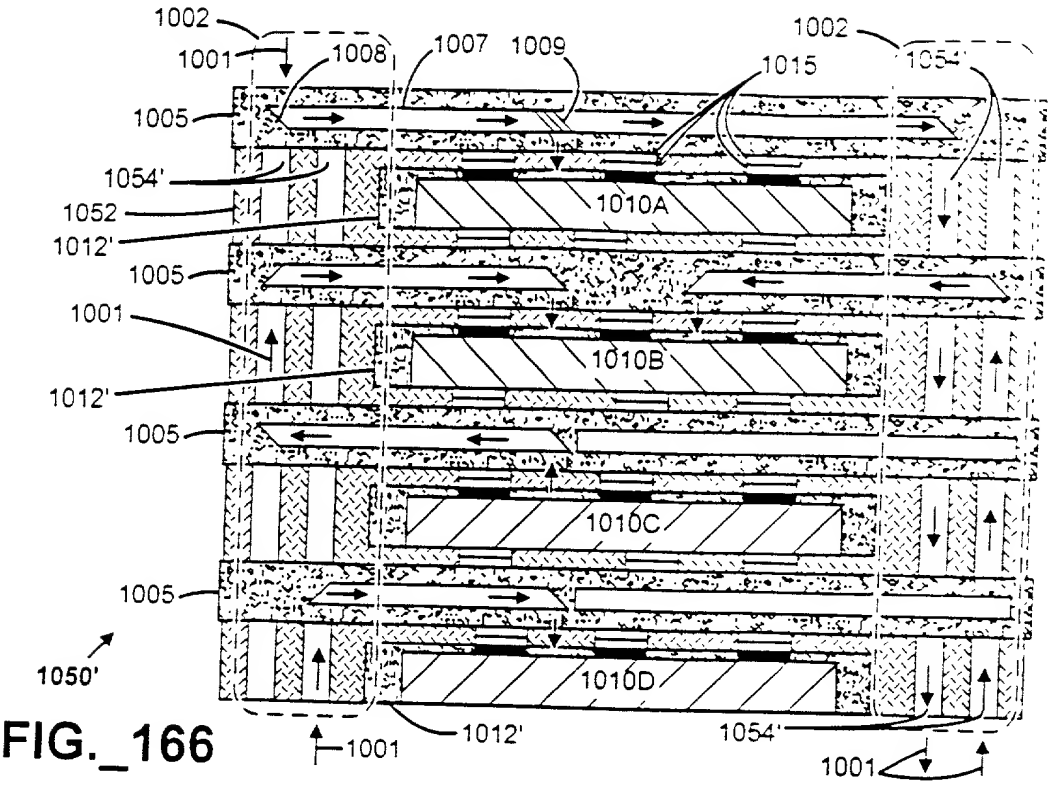


FIG._166

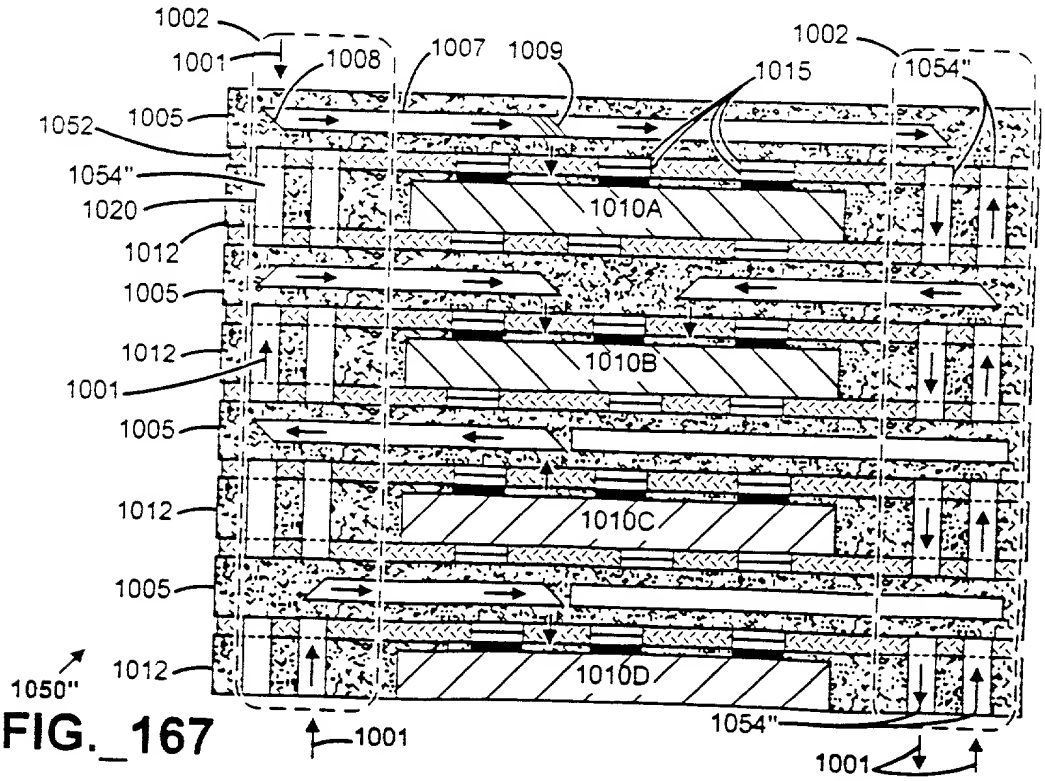


FIG._167

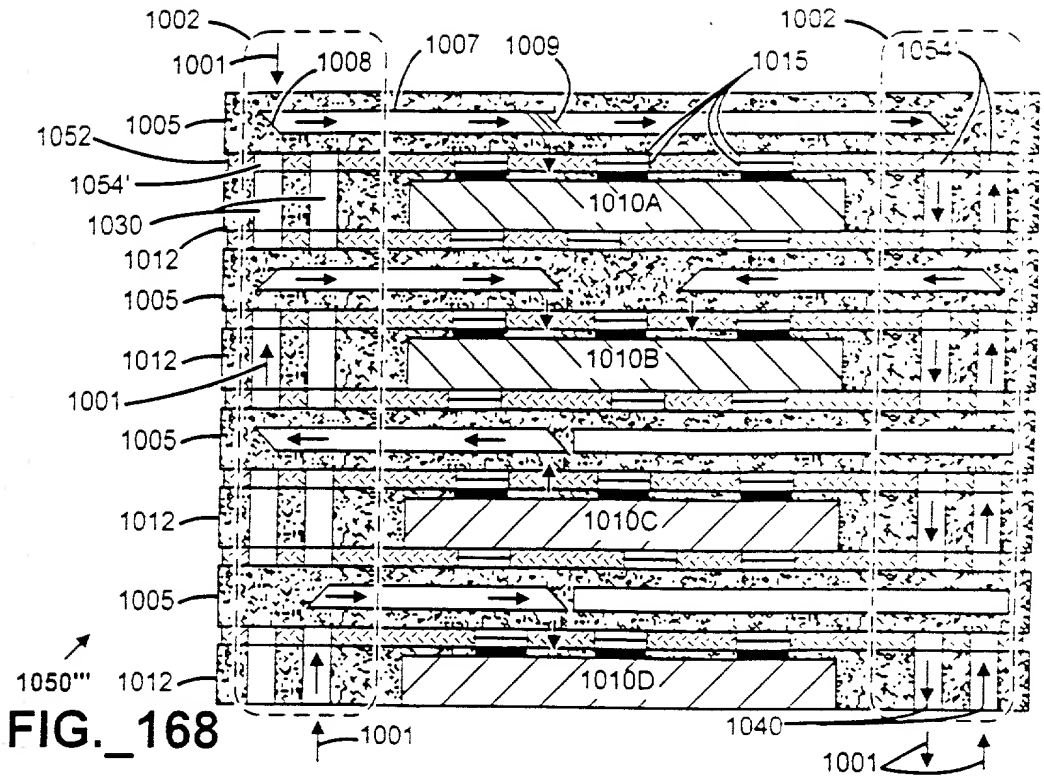


FIG._168

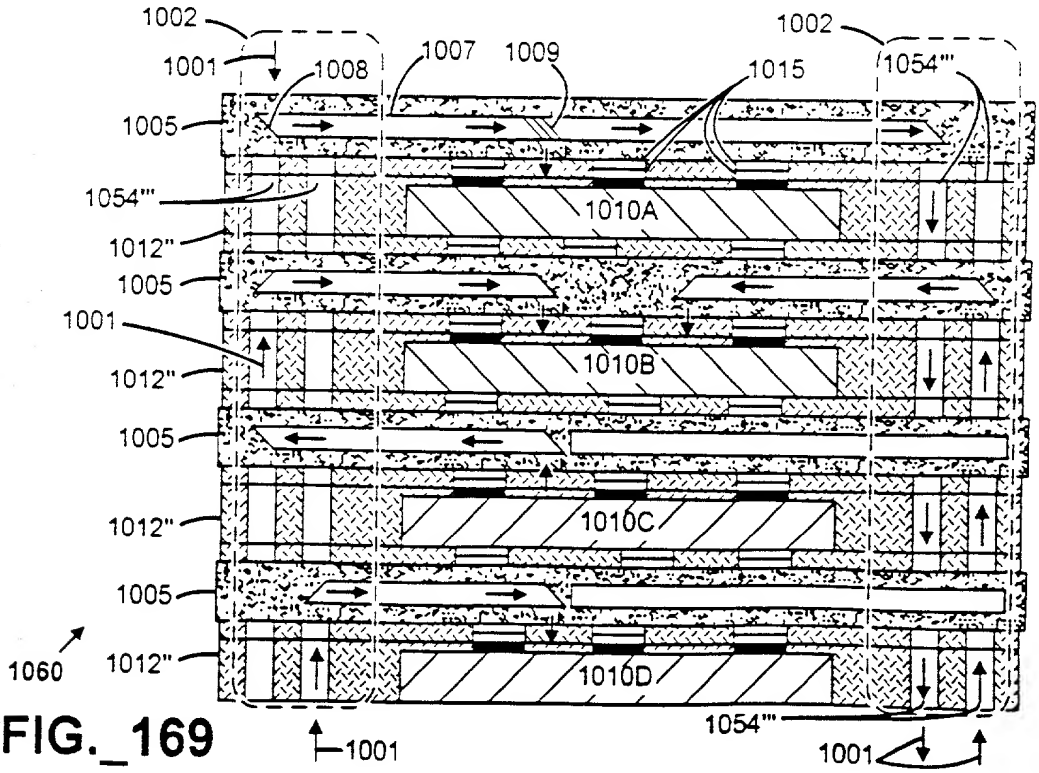


FIG._169

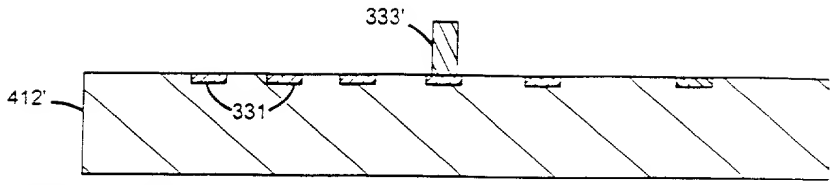


FIG._170

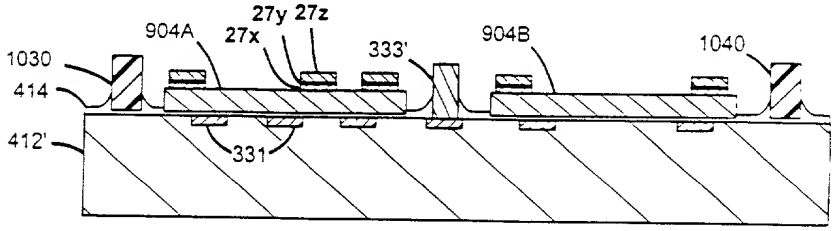


FIG._171

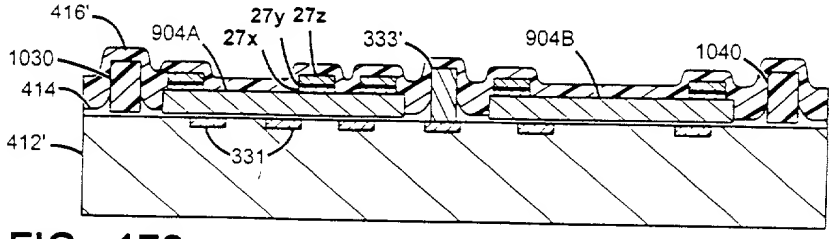


FIG._172

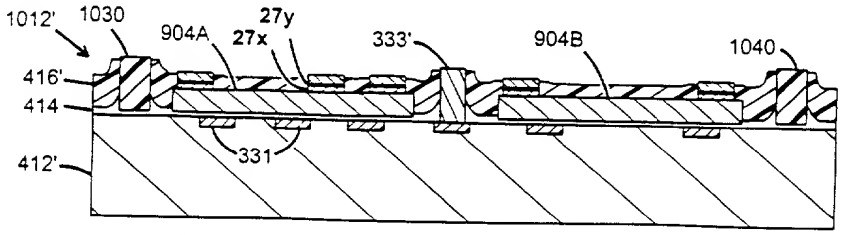


FIG._173

FUJITSU Computer Packaging Technologies, Inc. FCPT

I/O Connection in OE Substrate (Planar Modulator)

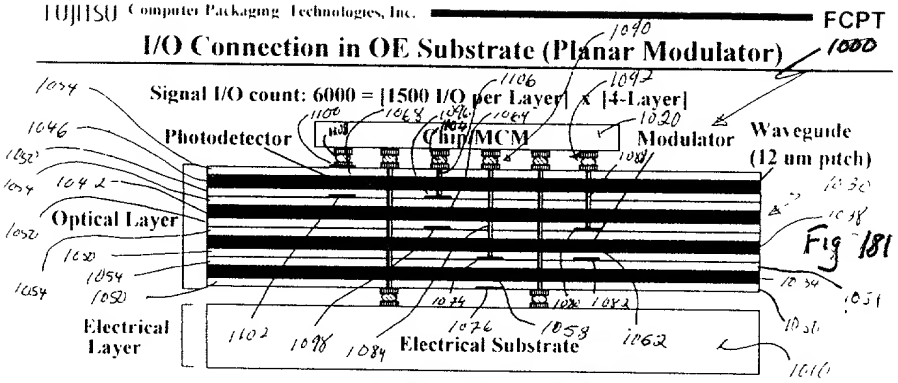


Fig 181

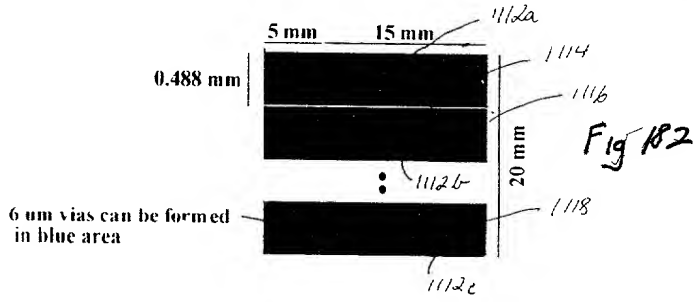


Fig 182

FUJITSU Computer Packaging Technologies, Inc. FCPT

I/O Connection in OE Substrate (Planar Modulator)

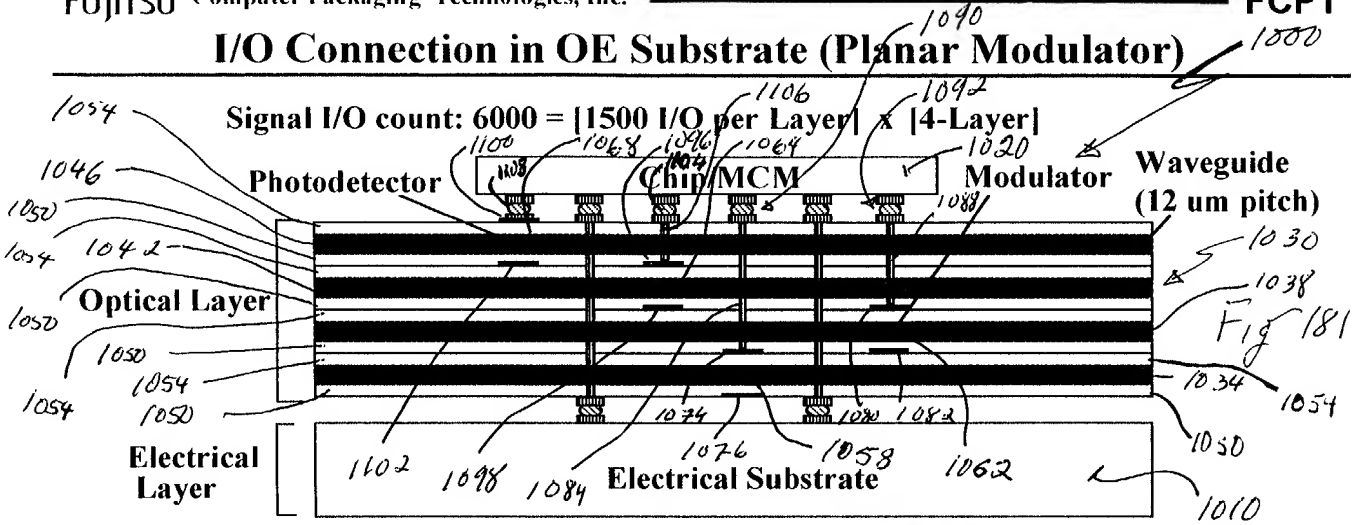


Fig 181

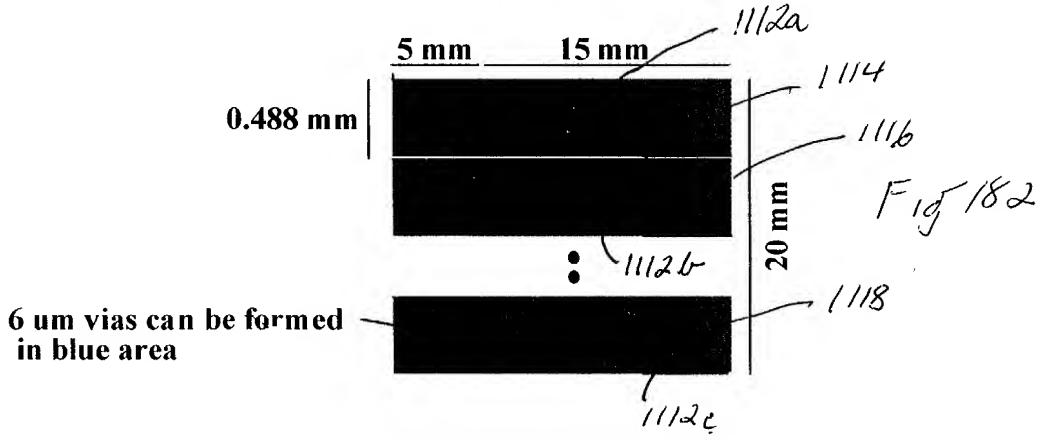


Fig 182

FUJITSU Computer Packaging Technologies, Inc. FCPT

I/O Connection in OE Substrate (Planar Modulator)

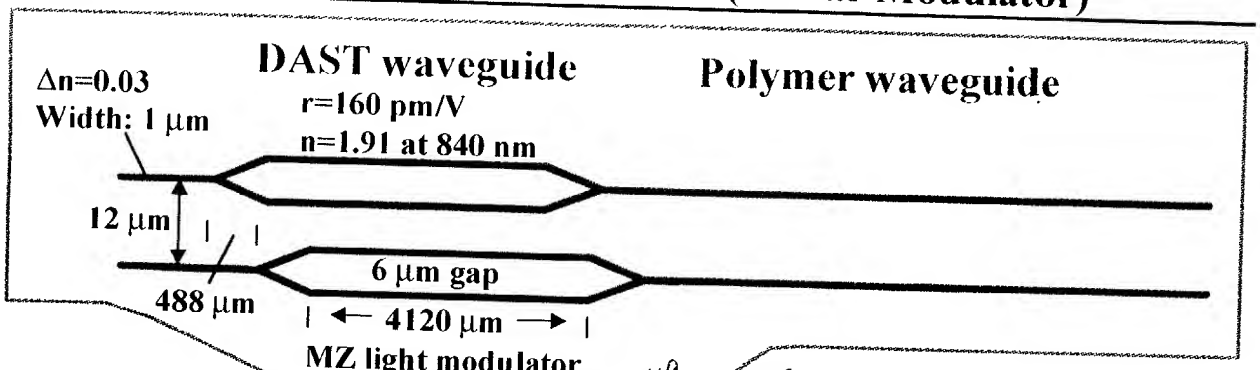
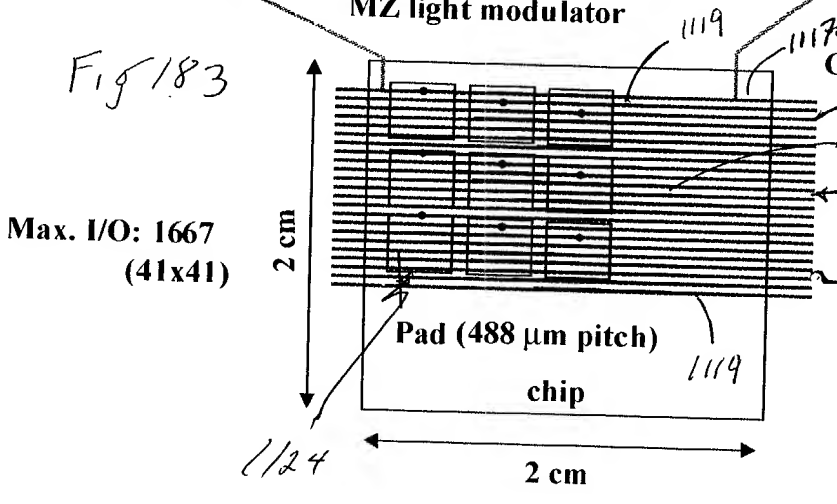


Fig 183



Cross section of light Modulator

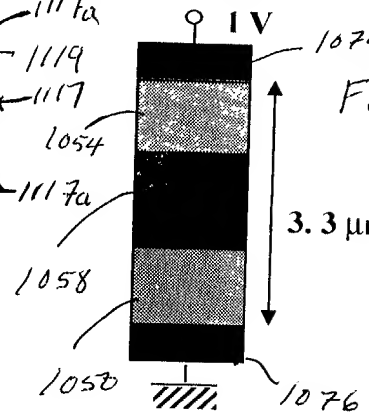


Fig 184

FUJITSU Computer Packaging Technologies, Inc. FCPT

I/O Connection in OE Substrate (OE-VLSI)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

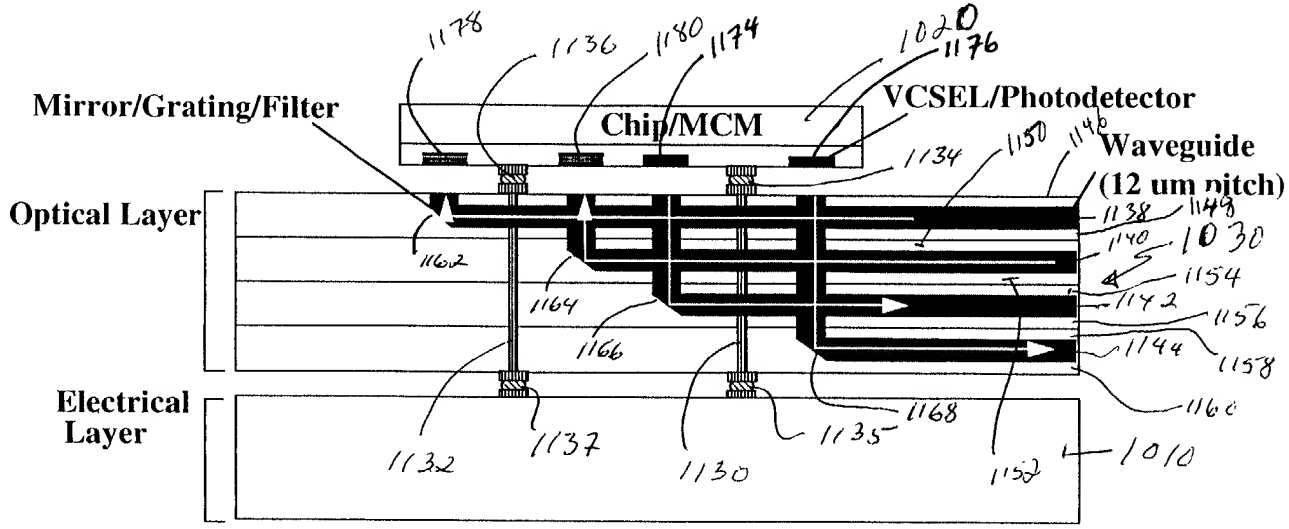


Fig 185

FUJITSU Computer Packaging Technologies, Inc. FCPT

I/O Connection in OE Substrate (OE-VLSI)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

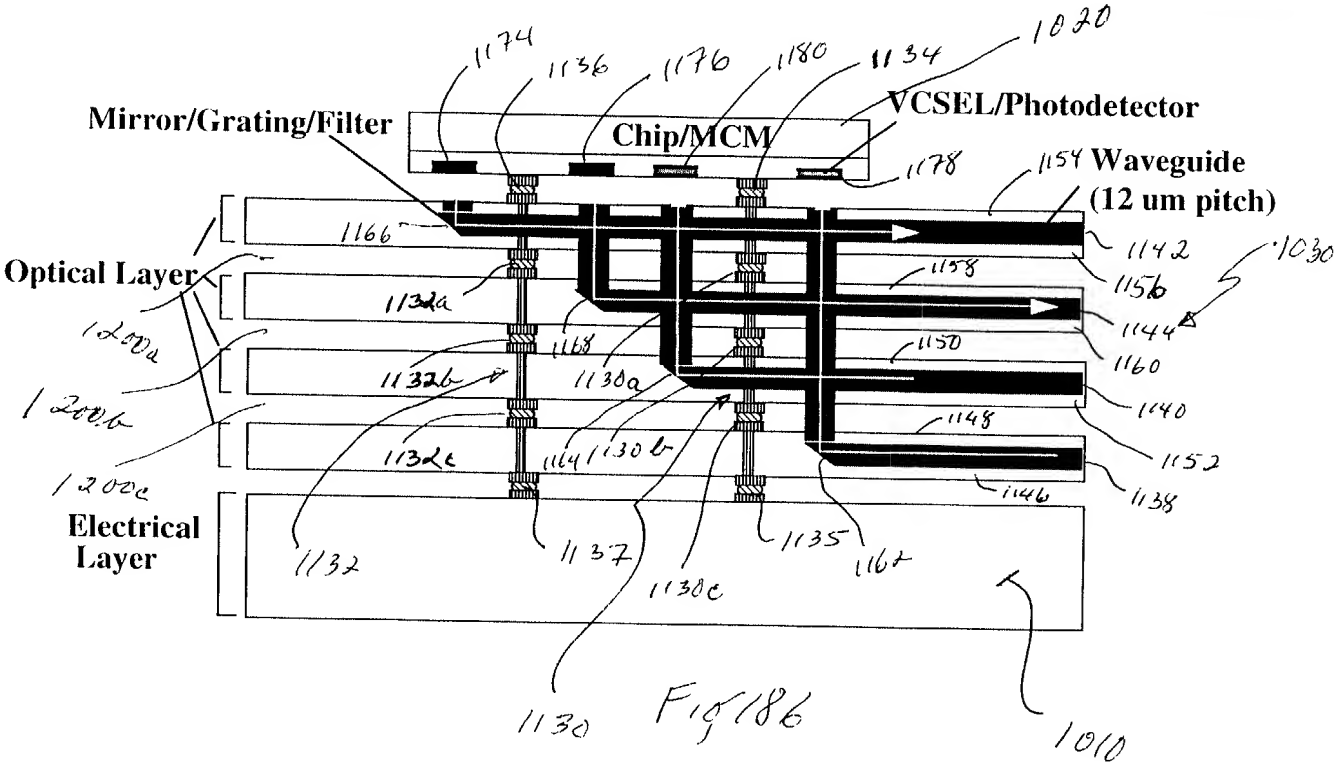


Fig 186

FUJITSU Computer Packaging Technologies, Inc. FCPT

I/O Connection in OE Substrate (OE-VLSI, WDM)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

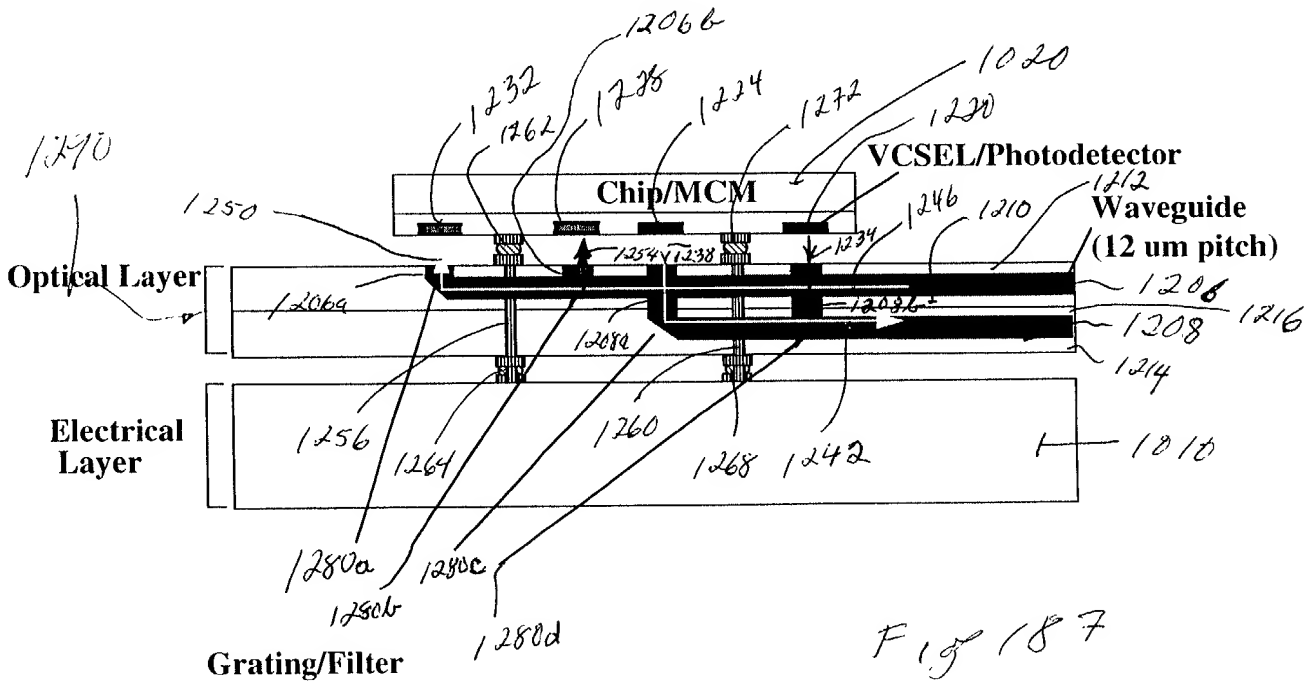


Fig 187

FUJITSU Computer Packaging Technologies, Inc. FCPT

I/O Connection in OE Substrate (OE-VLSI, WDM)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

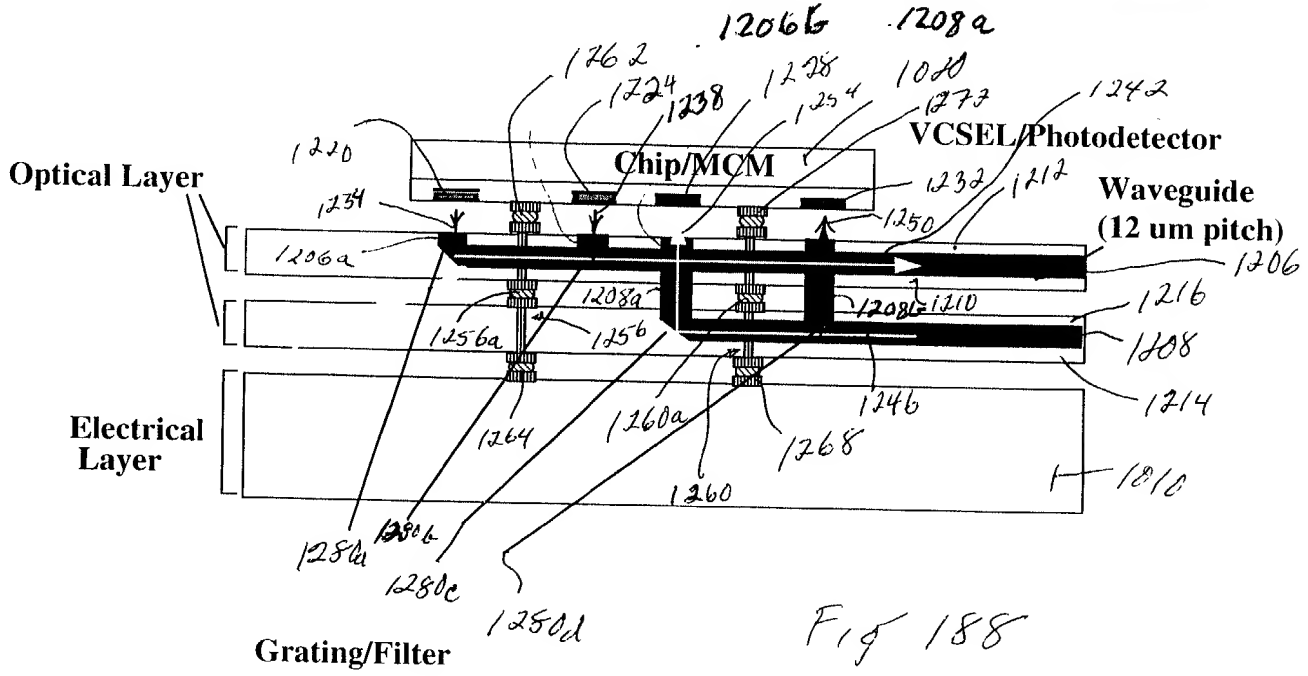


Fig 18B

FUJITSU Computer Packaging Technologies, Inc. FCPT

I/O Connection in OE Substrate (Active OE Layer)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

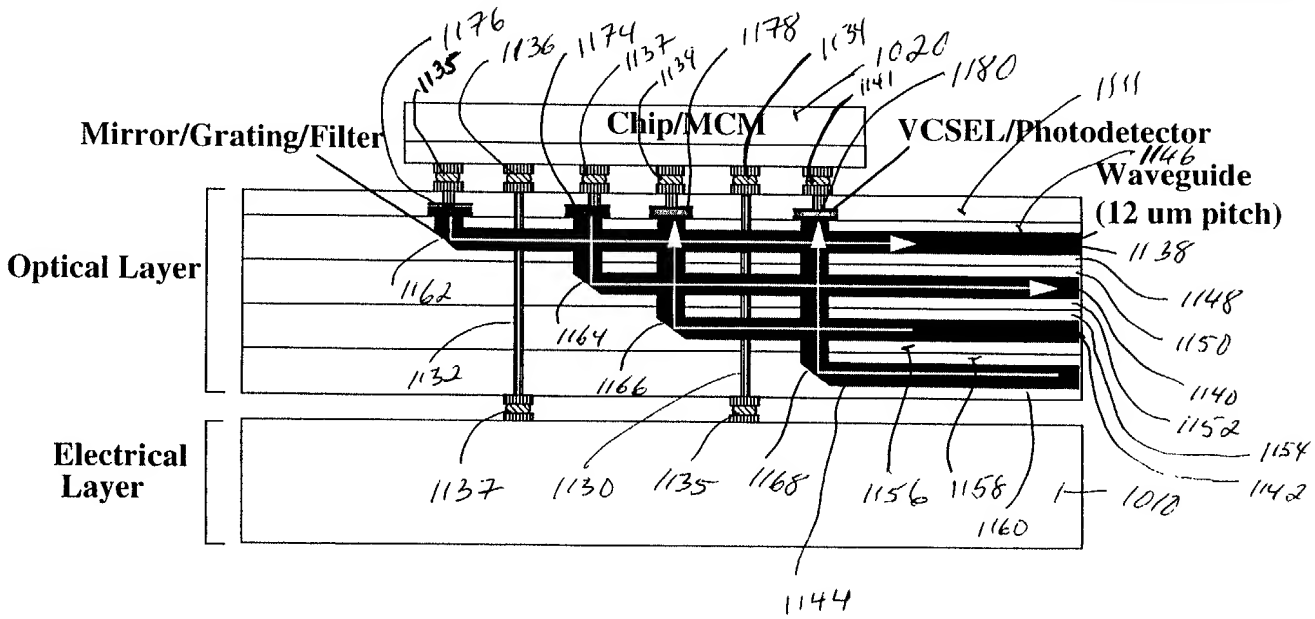


Fig 189

FUJITSU Computer Packaging Technologies, Inc. FCPT

I/O Connection in OE Substrate (Active OE Layer)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

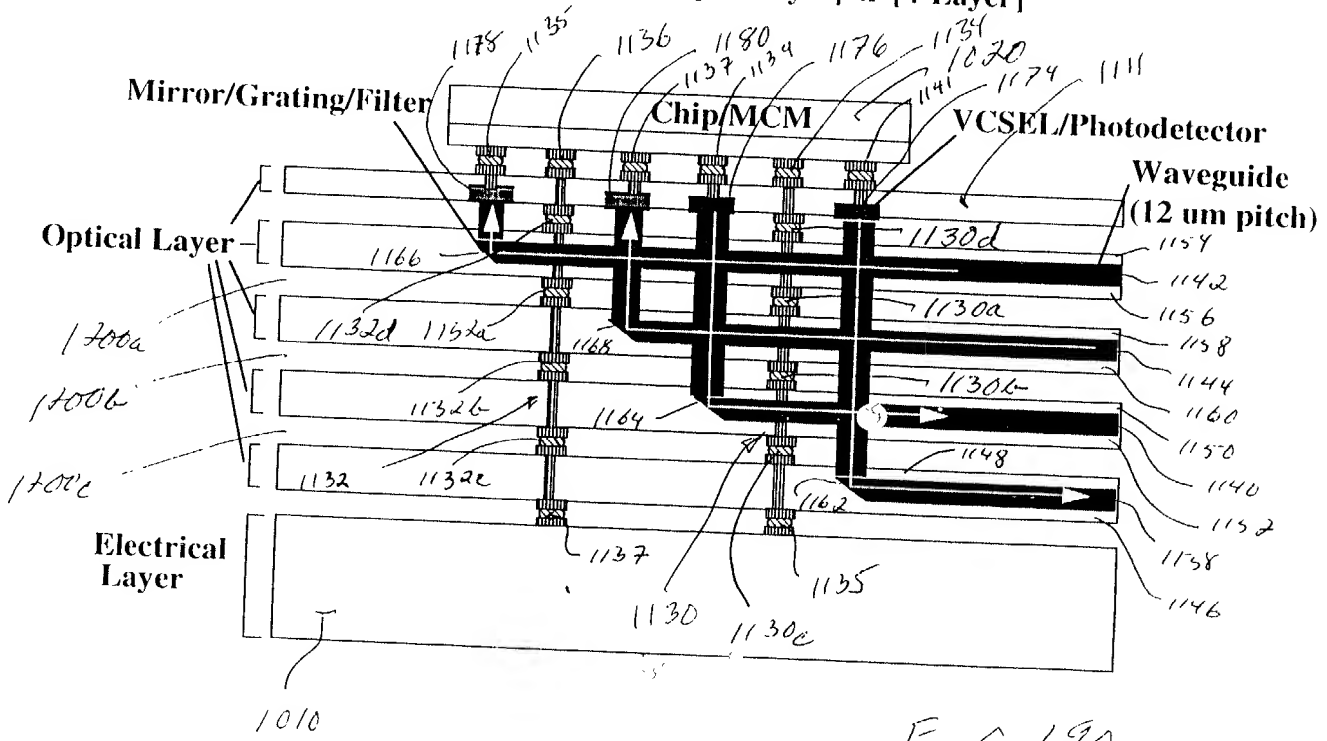


Fig 190

FUJITSU Computer Packaging Technologies, Inc. FCPT

I/O Connection in OE Substrate (Active OE Layer , WDM)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

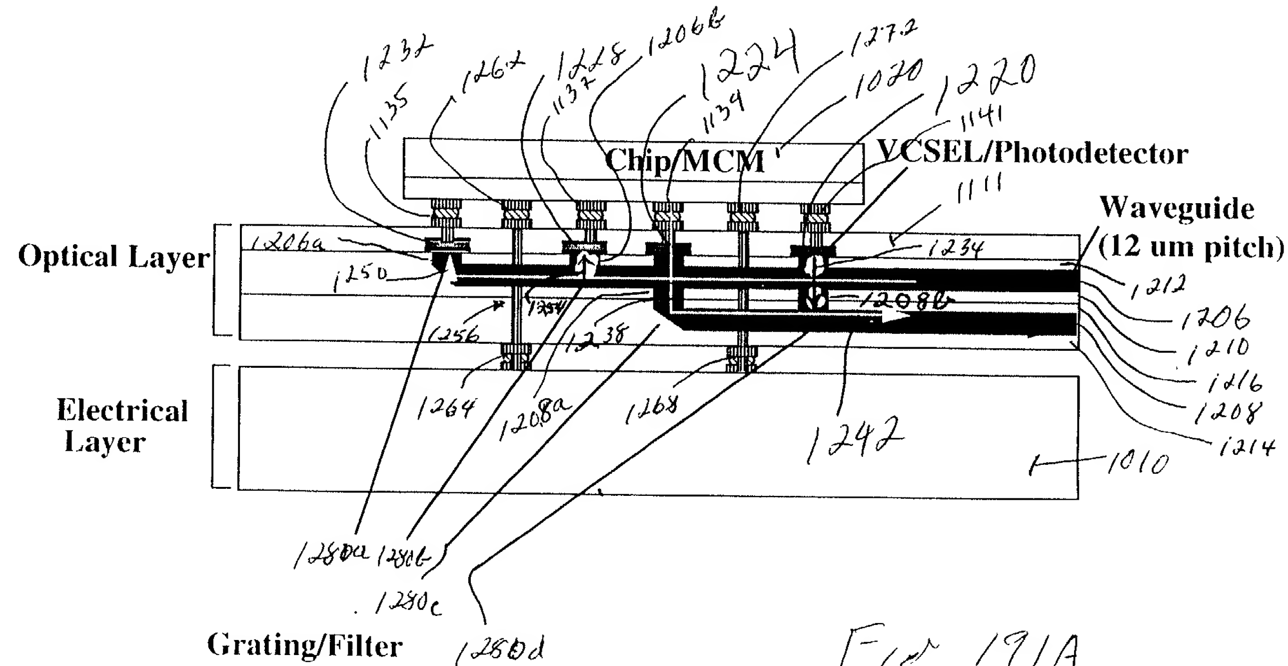


Fig 19A

FUJITSU Computer Packaging Technologies, Inc. FCPT

I/O Connection in OE Substrate (Active OE Layer , WDM)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

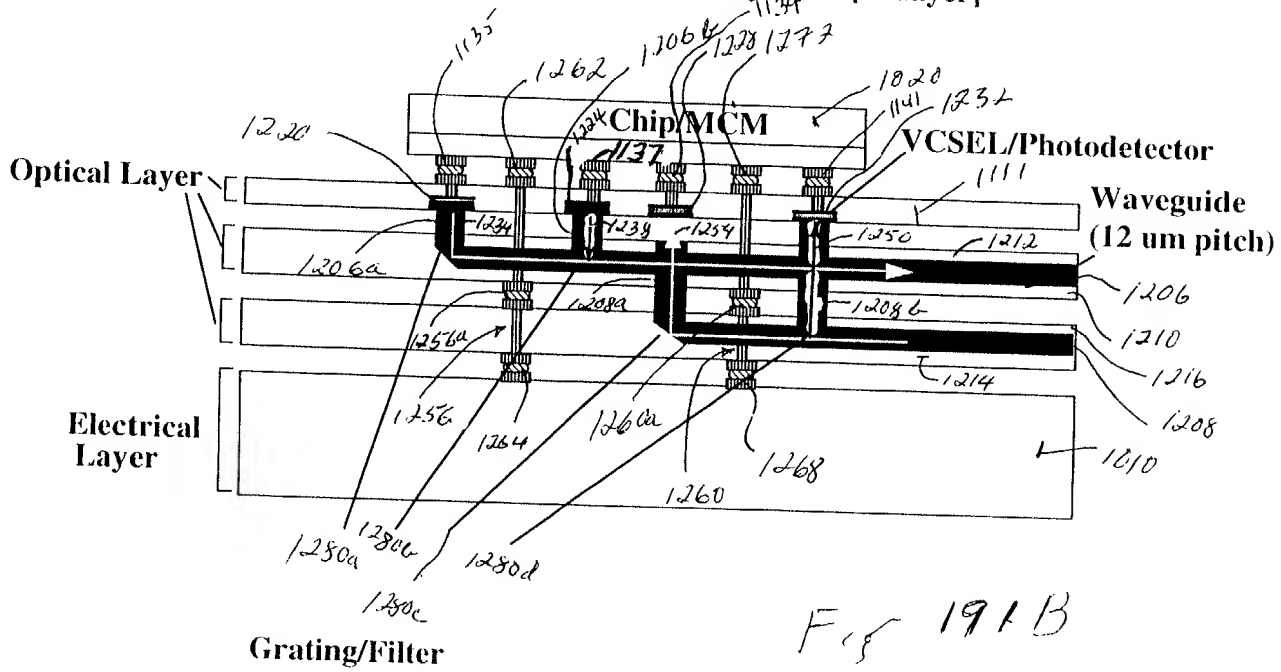


Fig 191B

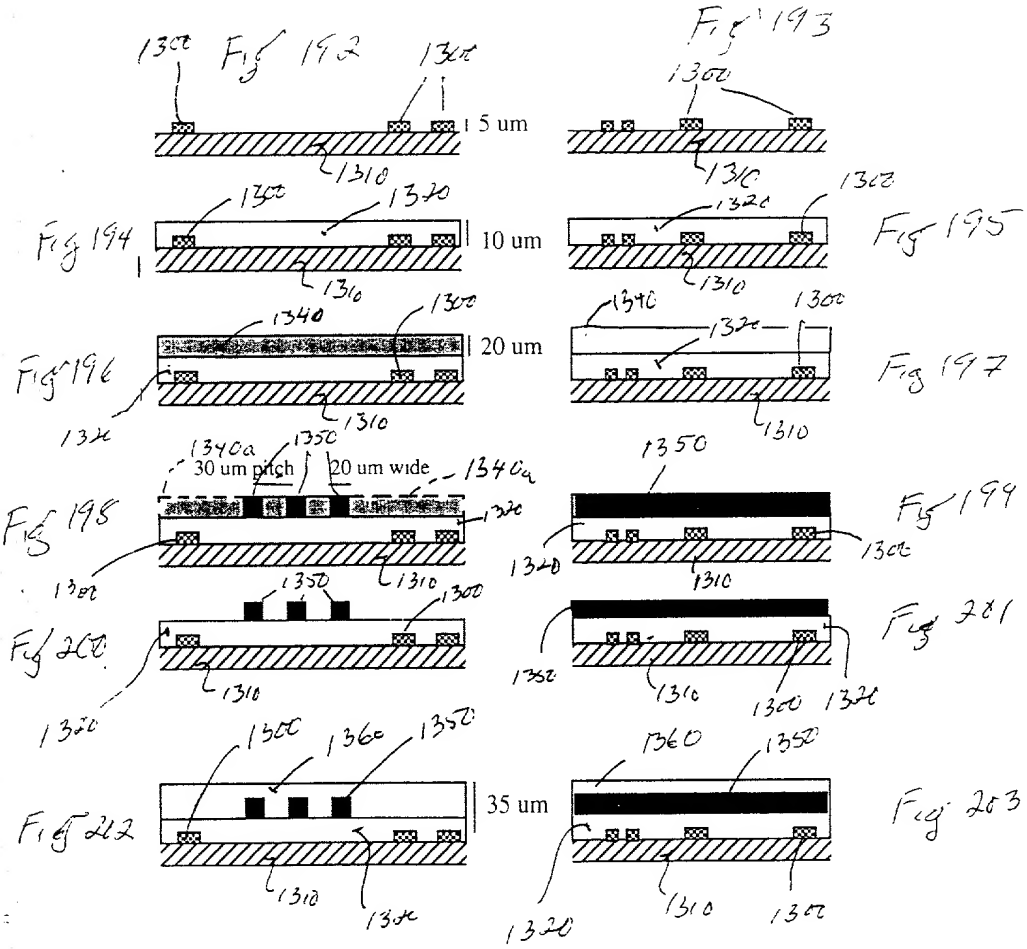
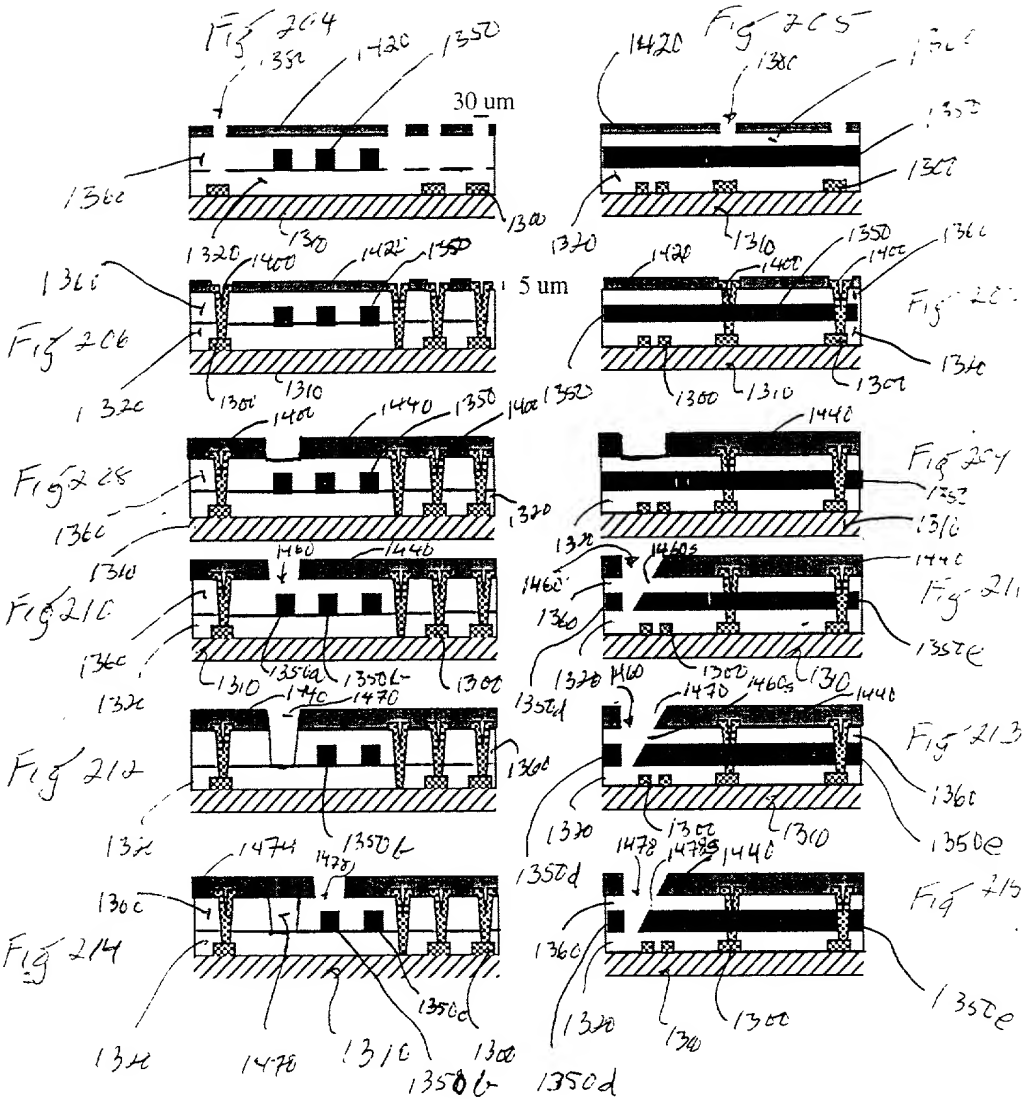


Fig 192
Fig 193
5 um
Fig 194
Fig 195
10 um
Fig 196
Fig 197
20 um
Fig 198
30 um pitch
20 um wide
Fig 199
Fig 200
Fig 201
Fig 202
35 um
Fig 203


30 um
5 um

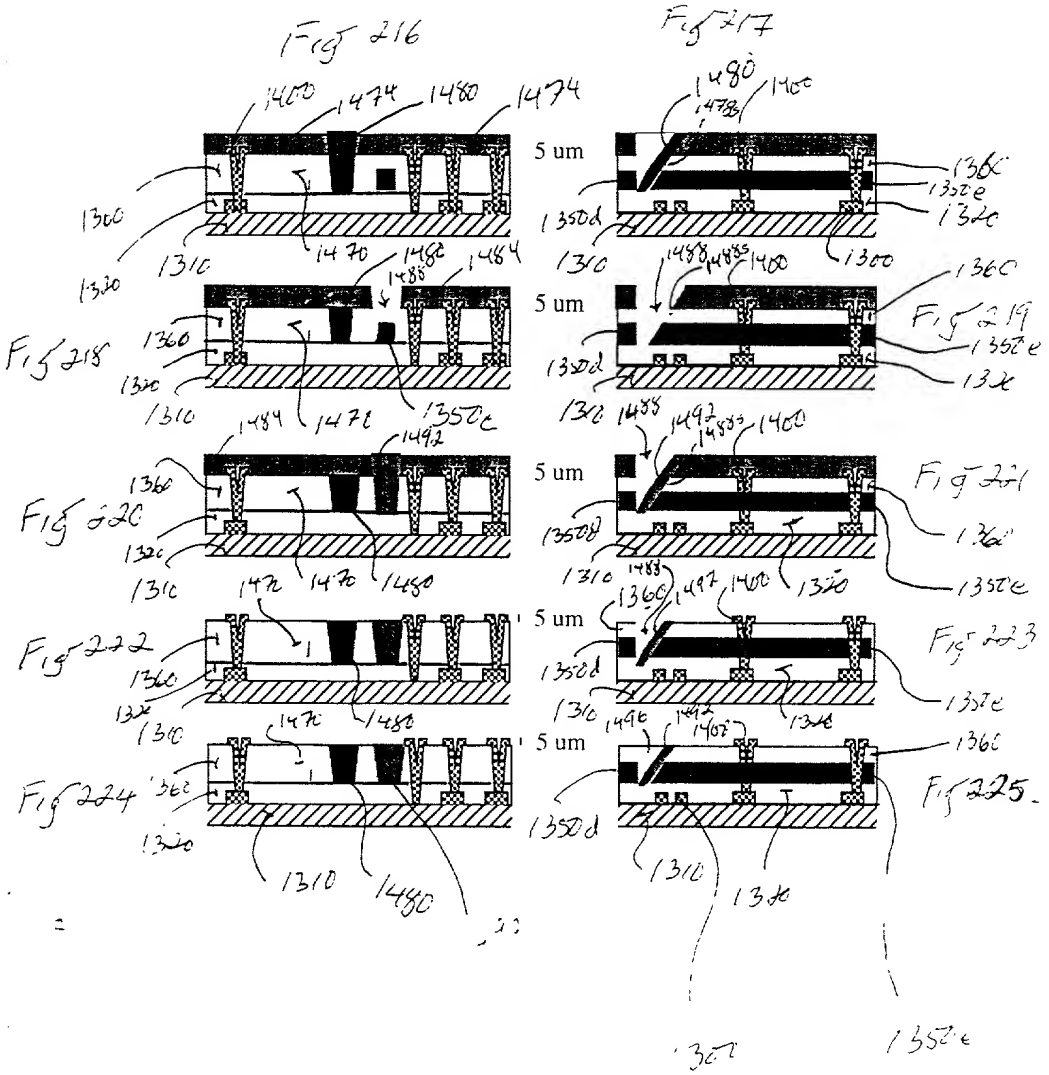


Fig 216
Fig 217
Fig 218
Fig 219
Fig 220
Fig 221
Fig 222
Fig 223
Fig 224
Fig 225
5 um
1400
1474
1480
1360
1310
1320
1470
1488
1484
1350e
1492
1350d
1496
1497
1300
1340
1350
1360

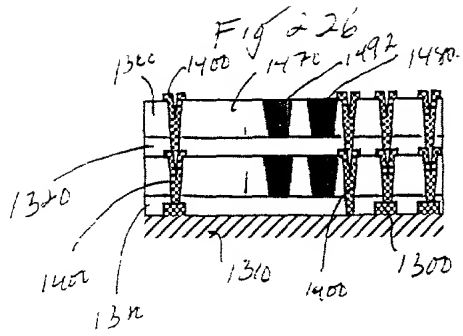


Fig 26

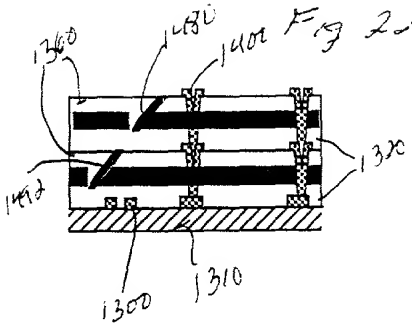


Fig 27

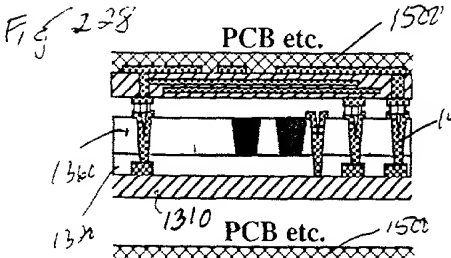


Fig 28

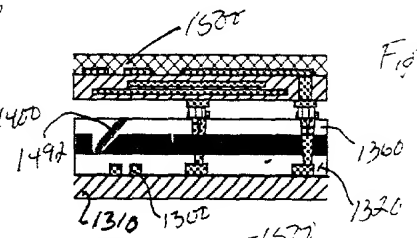


Fig 29

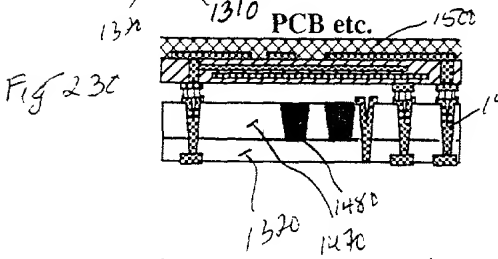


Fig 30

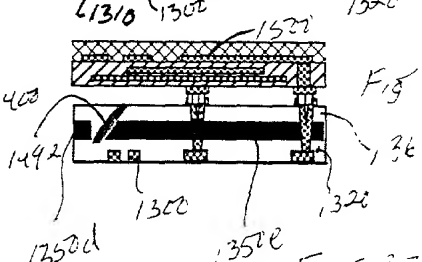


Fig 31

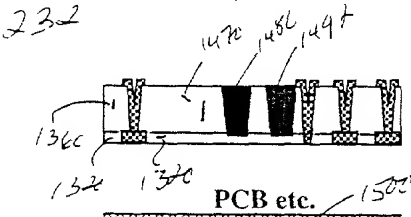


Fig 32

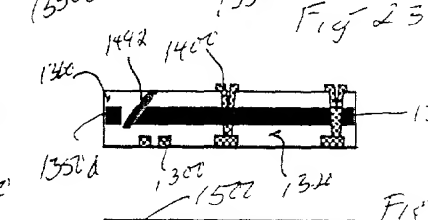


Fig 33

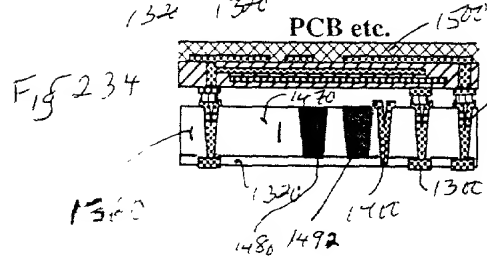


Fig 34

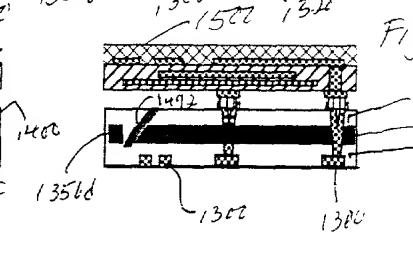


Fig 35

Fig 236

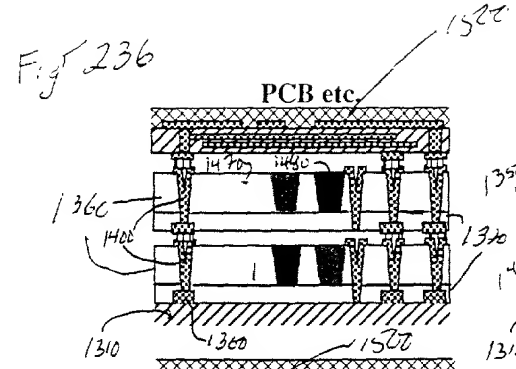


Fig 237

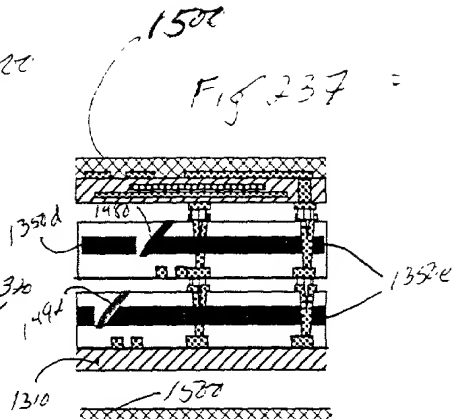


Fig 238

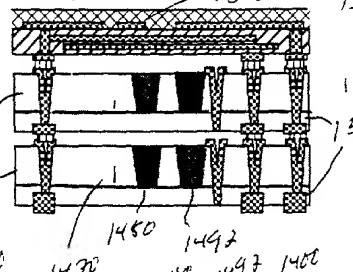


Fig 239

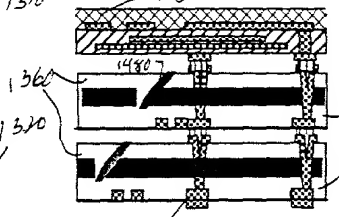


Fig 240

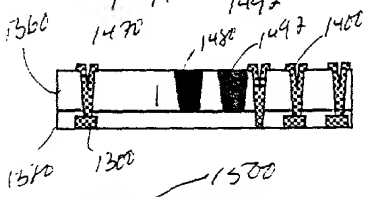


Fig 241

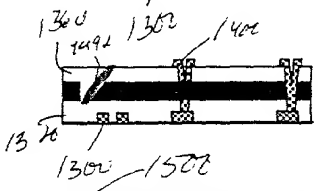


Fig 242

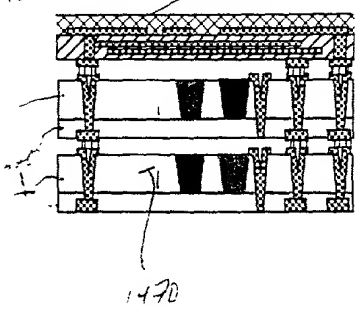


Fig 243

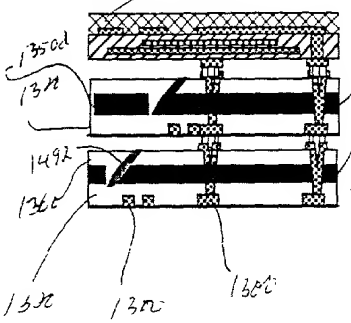


Fig 244

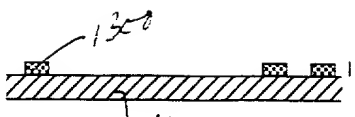


Fig 245

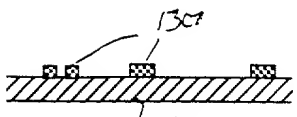


Fig 246

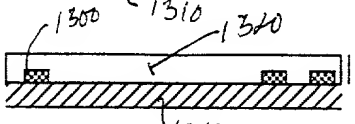


Fig 247

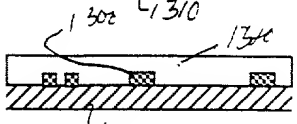


Fig 248

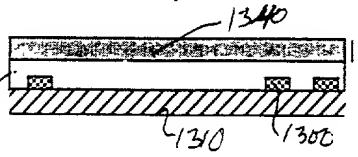


Fig 249

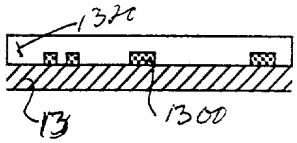


Fig 250

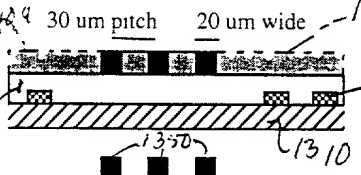


Fig 251

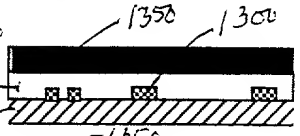


Fig 252

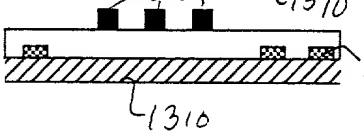


Fig 253

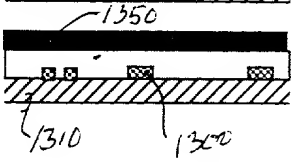


Fig 254

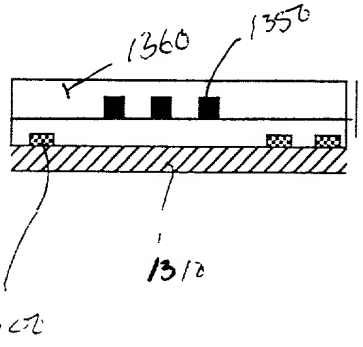
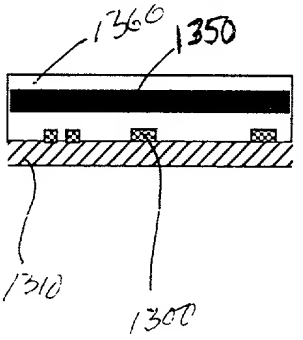
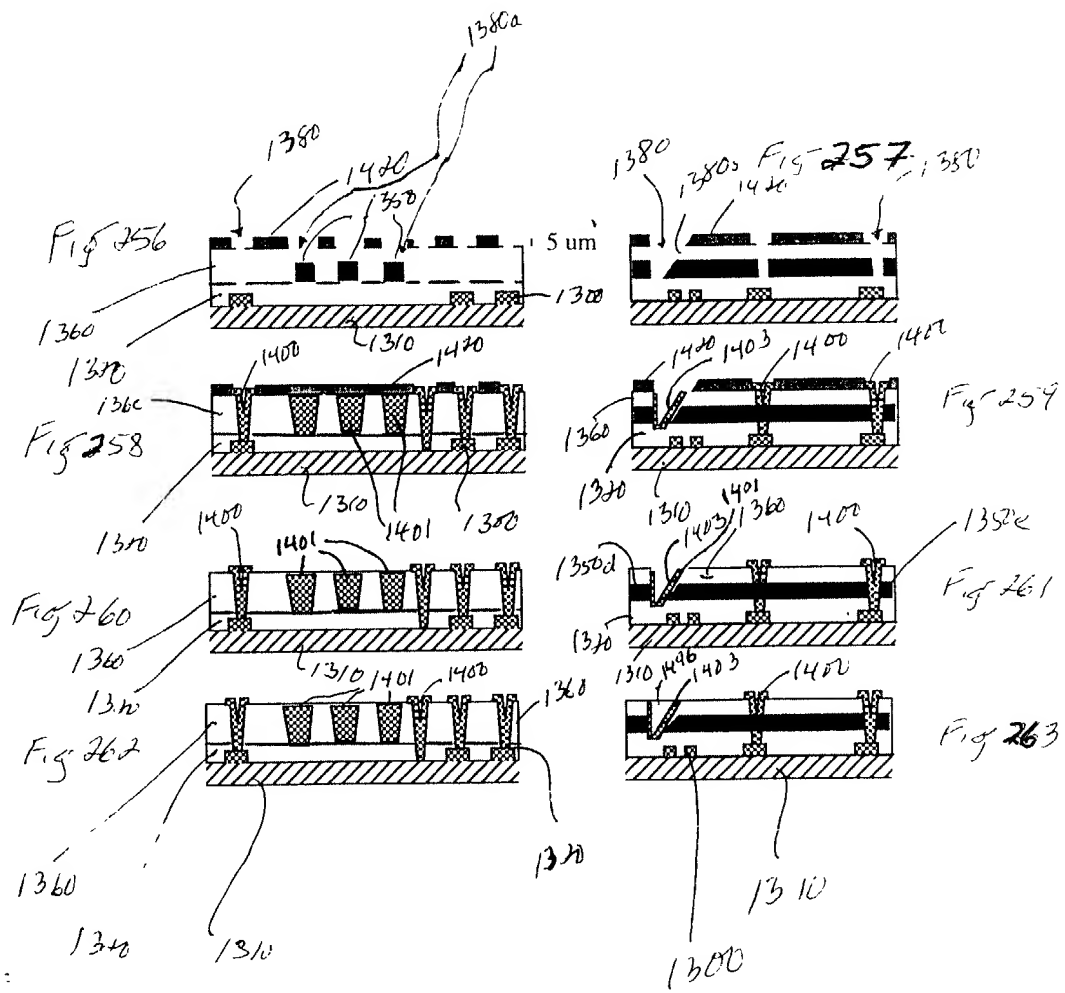


Fig 255




1380a
1380
1420
1350
5 um
1300
1360
1370
1310
1400
1420
1401
1403
1350d
1350c
1496
Fig 256
Fig 257
Fig 258
Fig 259
Fig 260
Fig 261
Fig 262
Fig 263

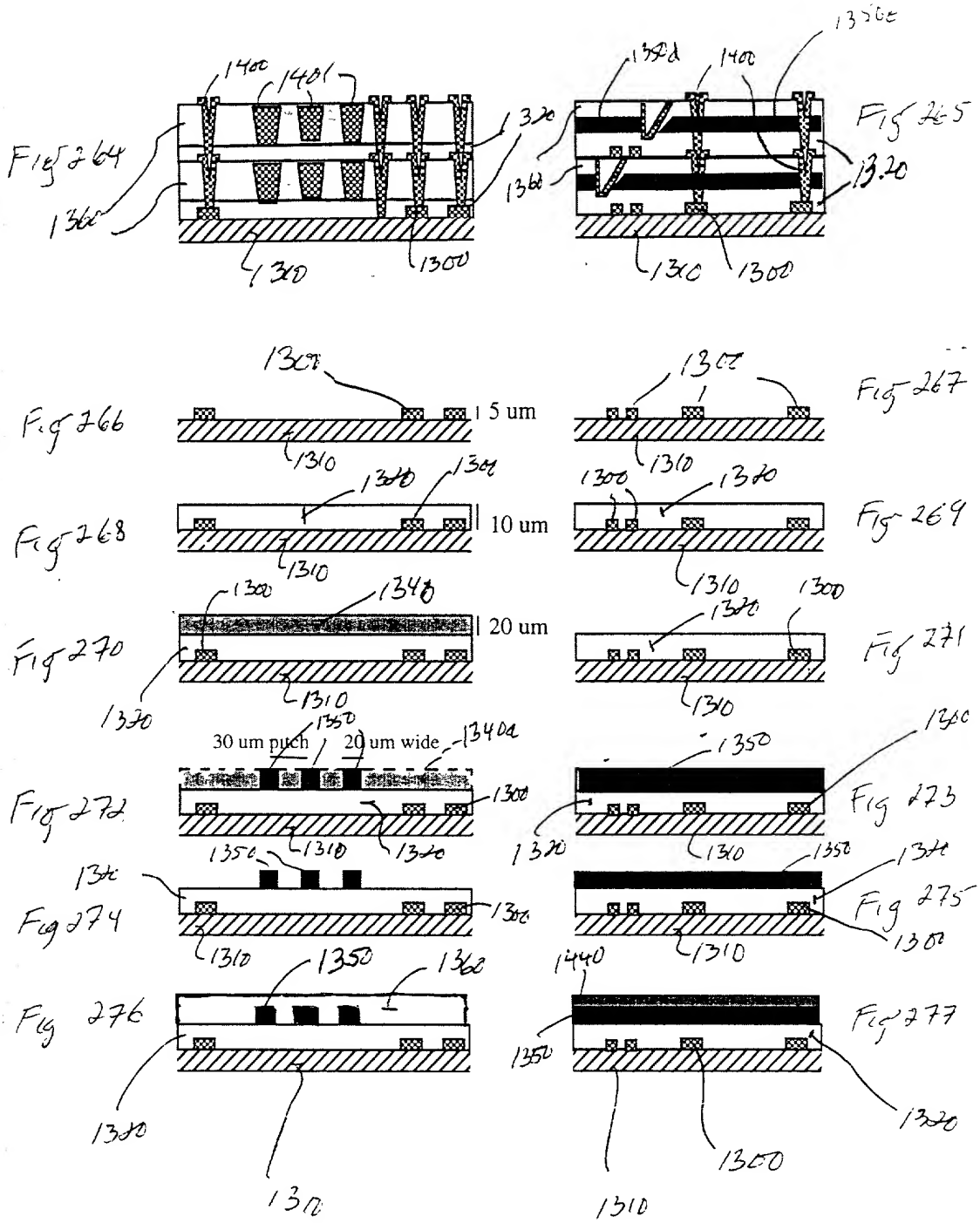


Fig 264
Fig 265
Fig 266
Fig 267
Fig 268
Fig 269
Fig 270
Fig 271
Fig 272
Fig 273
Fig 274
Fig 275
Fig 276
Fig 277
15 um
10 um
20 um
30 um pitch
20 um wide

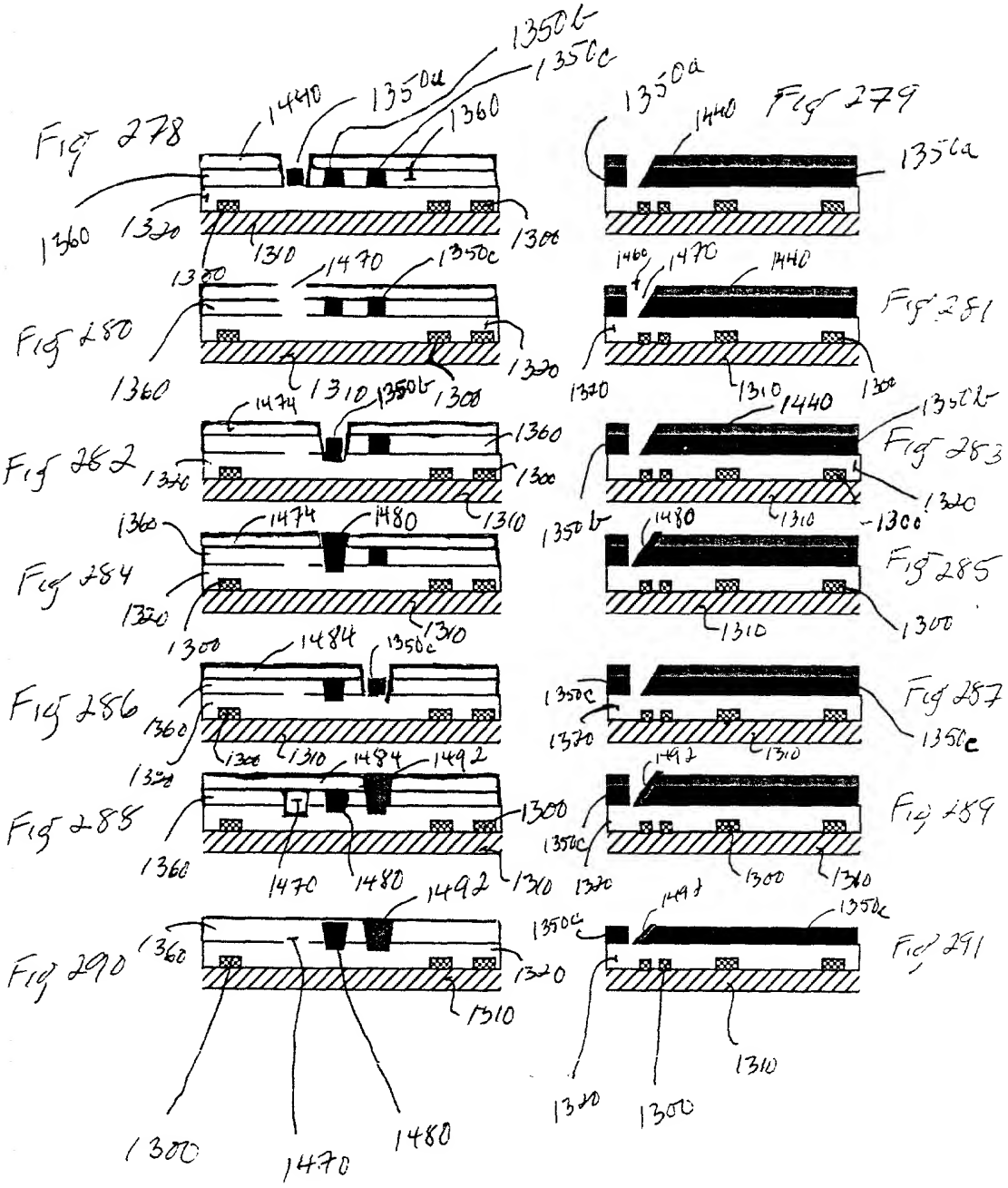
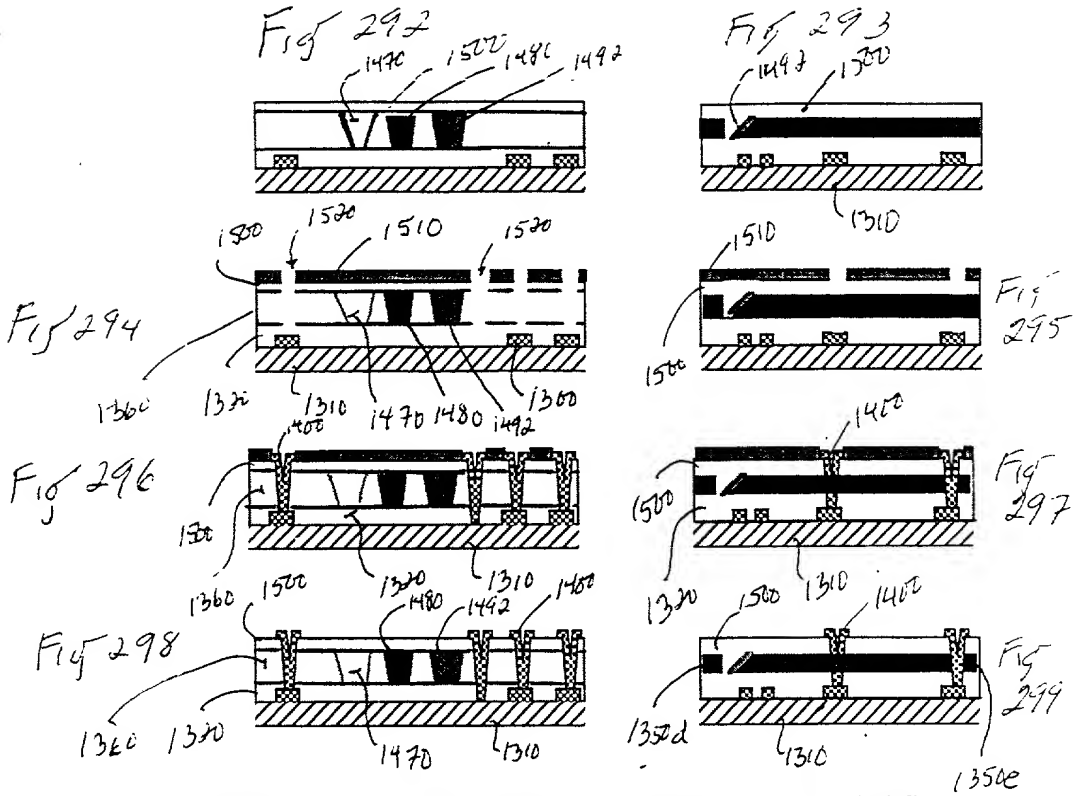
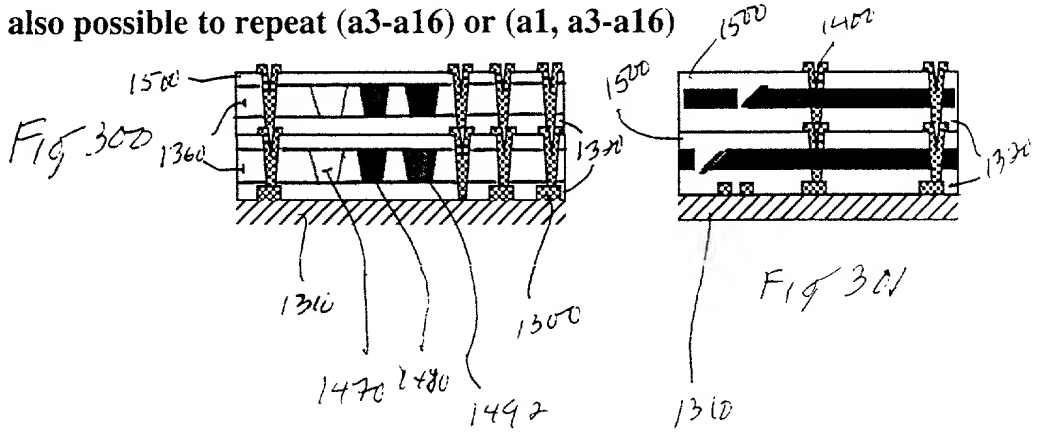


Fig 278
1440
1350a
1350b
1350c
1360
1360
1320
1310
1300
Fig 279
1350a
1440
Fig 280
1320
1470
1350c
1360
1310
1350b
1300
Fig 281
1460
1470
1440
1370
1310
1300
Fig 282
1474
1360
1320
1300
1310
Fig 283
1350b
1440
1320
1310
1300
Fig 284
1360
1474
1480
1320
1300
1310
Fig 285
1480
1310
1300
Fig 286
1484
1350c
1360
1320
1300
1310
Fig 287
1350c
1370
1310
1350c
Fig 288
1484
1492
1360
1470
1480
1492
1300
1310
Fig 289
1492
1350c
1370
1300
1310
Fig 290
1360
1320
1310
1300
1470
1480
Fig 291
1492
1350c
1350c
1370
1300
1310



In the case of multi layer (a1-a16) process is repeated on the (a16).
-it is also possible to repeat (a3-a16) or (a1, a3-a16)



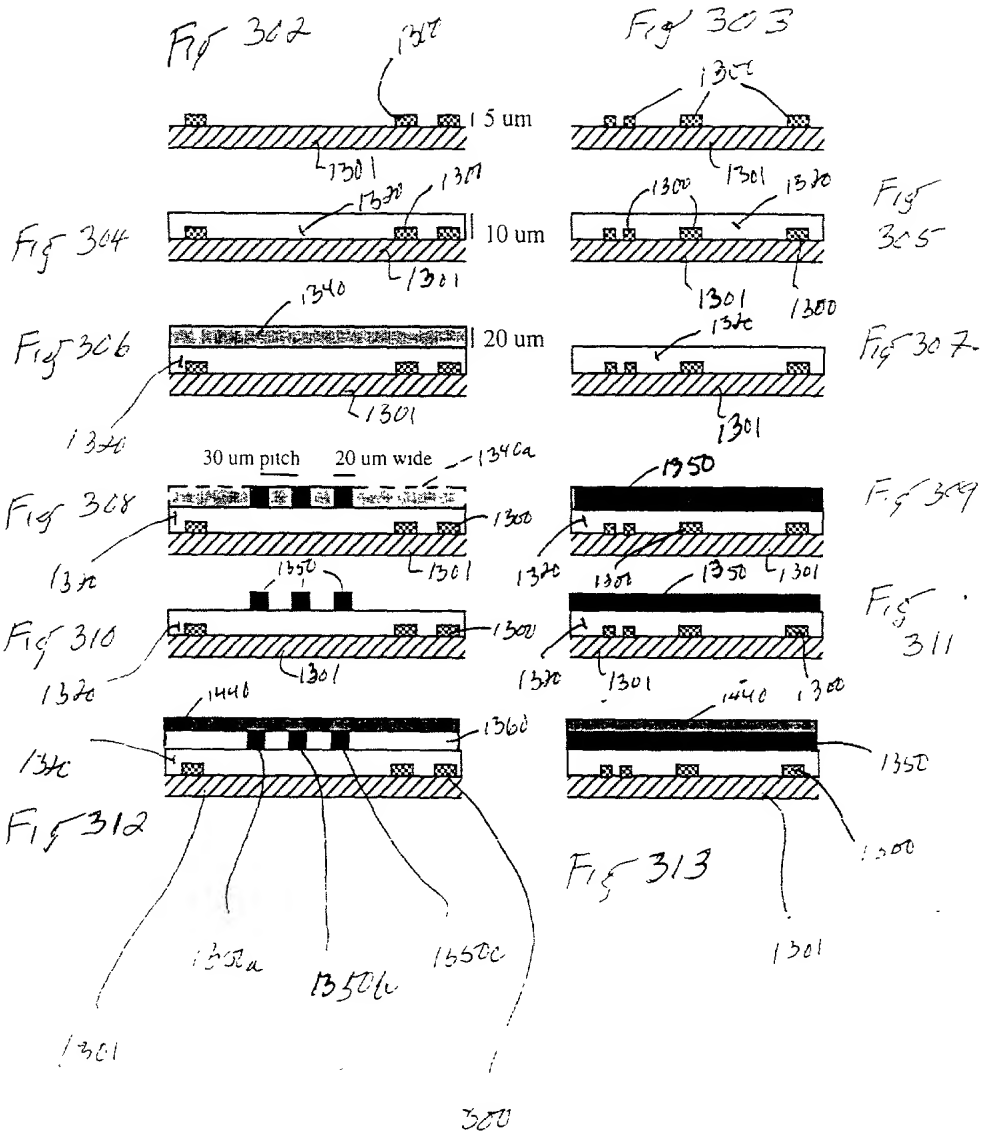


Fig 302
5 um
Fig 303
Fig 304
10 um
Fig 305
Fig 306
20 um
Fig 307
30 um pitch
20 um wide
Fig 308
Fig 309
Fig 310
Fig 311
Fig 312
Fig 313

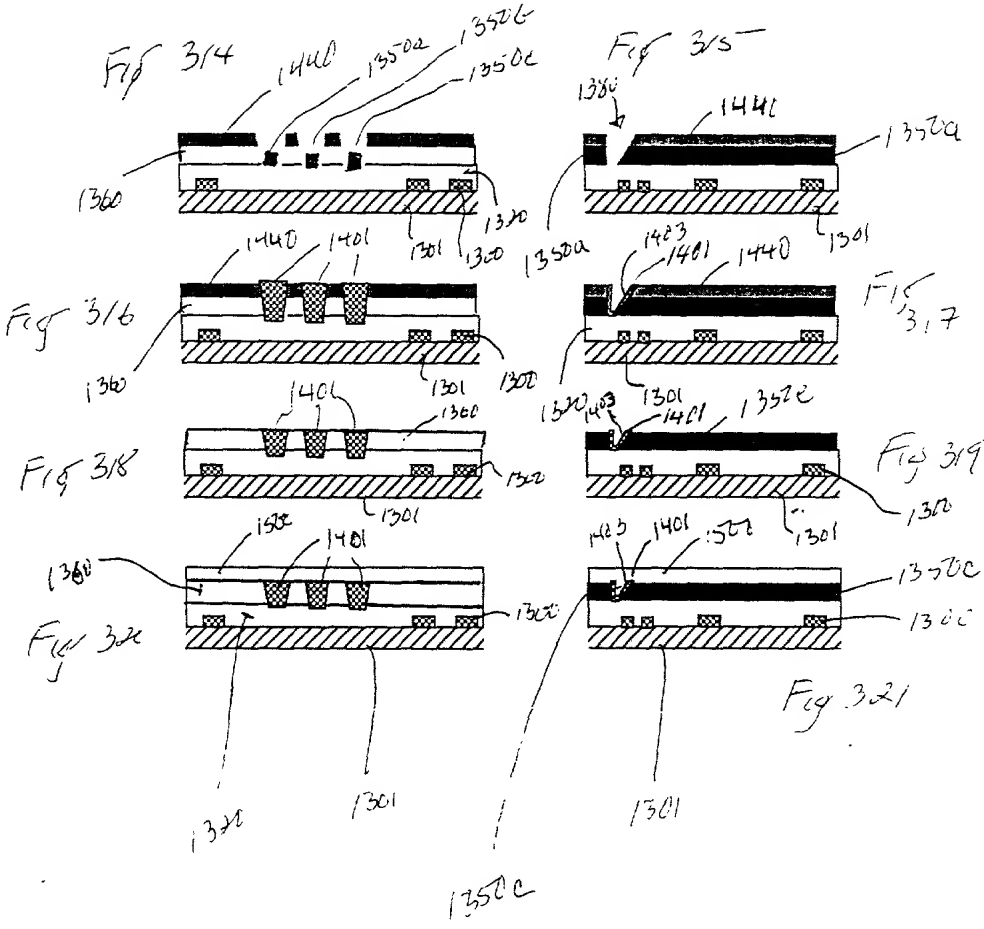
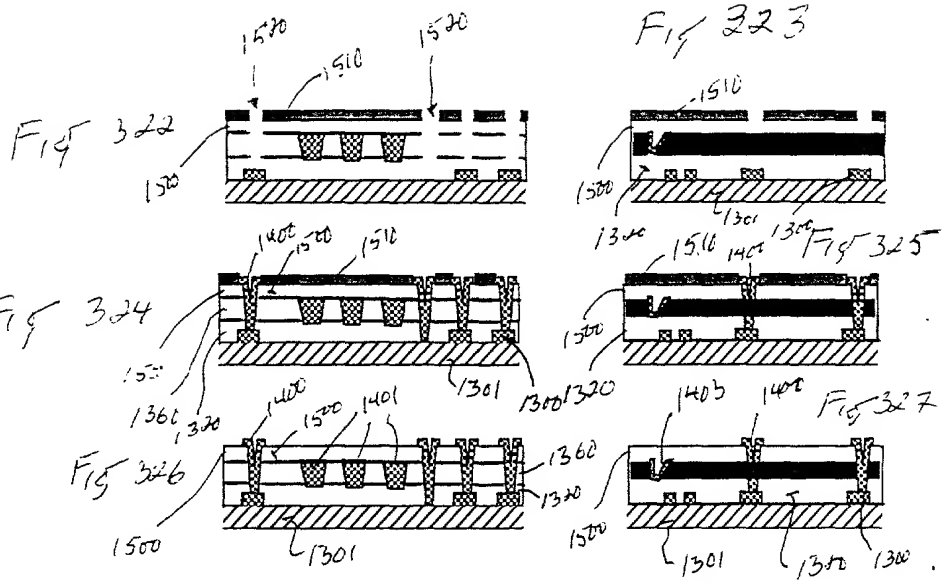
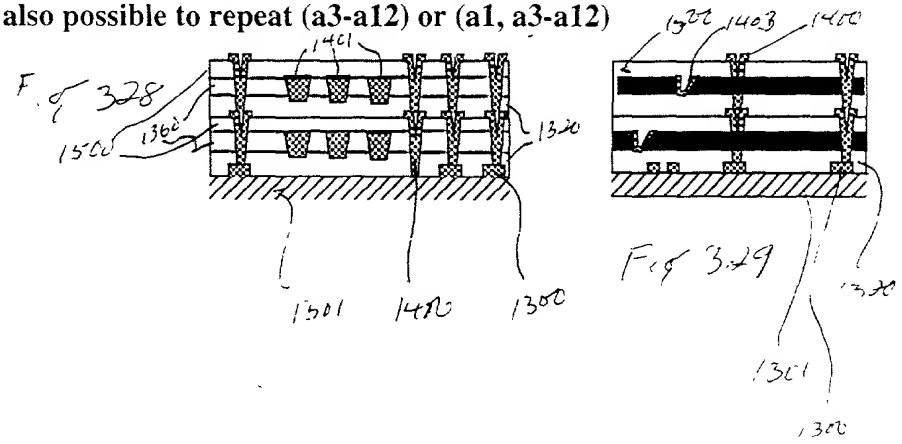


Fig 3/4
1440
1350a
1350c
1360
1301
1320
Fig 3/5
1360
1440
1350a
1301
1350a
1403
1401
1440
Fig 3/6
1440
1401
1360
1301
1320
Fig 3/7
1320
1403
1301
1401
1350c
Fig 3/8
1401
1360
1320
1301
Fig 3/9
1320
1301
1350c
1360
1401
1301
Fig 3/10
1403
1401
1350c
1350a
1300
Fig 3/11
1320
1301
1350c
1301



In the case of multi layer (a1-a12) process is repeated on the (a12).
-it is also possible to repeat (a3-a12) or (a1, a3-a12)



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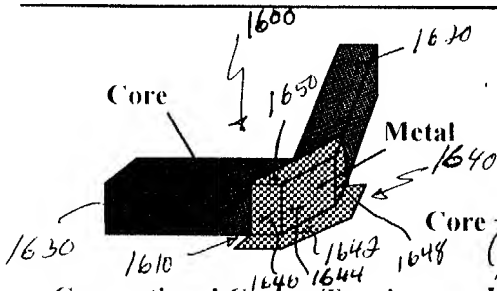
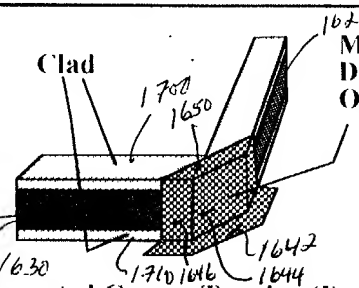
Conventional and Invented Waveguide Structure Examples



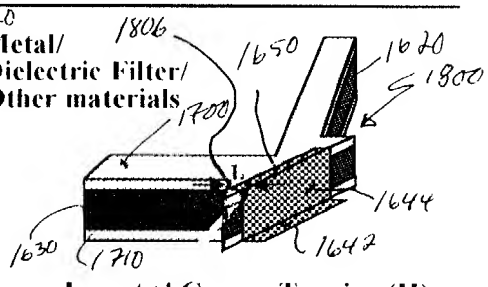
Conventional Corner Turning

Fig 330



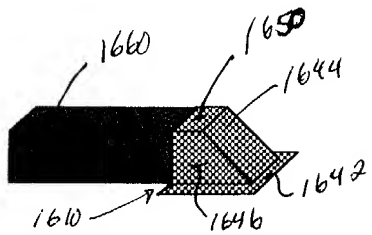
Invented Corner Turning (I)

Fig 332



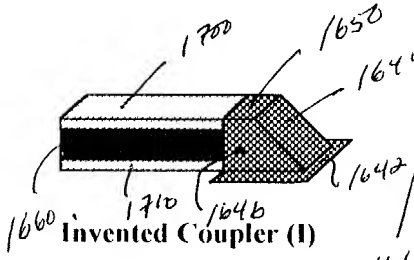
Invented Corner Turning (II)

Fig 334



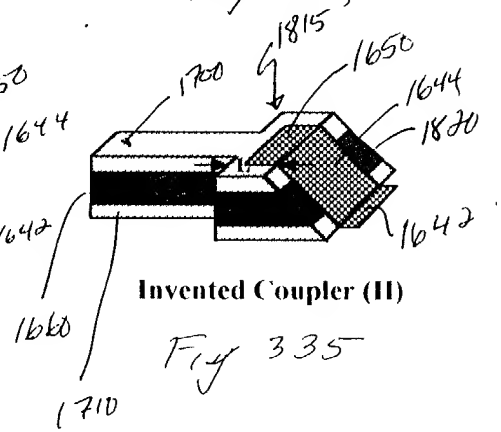
Conventional Coupler

Fig 331



Invented Coupler (I)

Fig 333



Invented Coupler (II)

Fig 335

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Conventional Corner Turning Structure

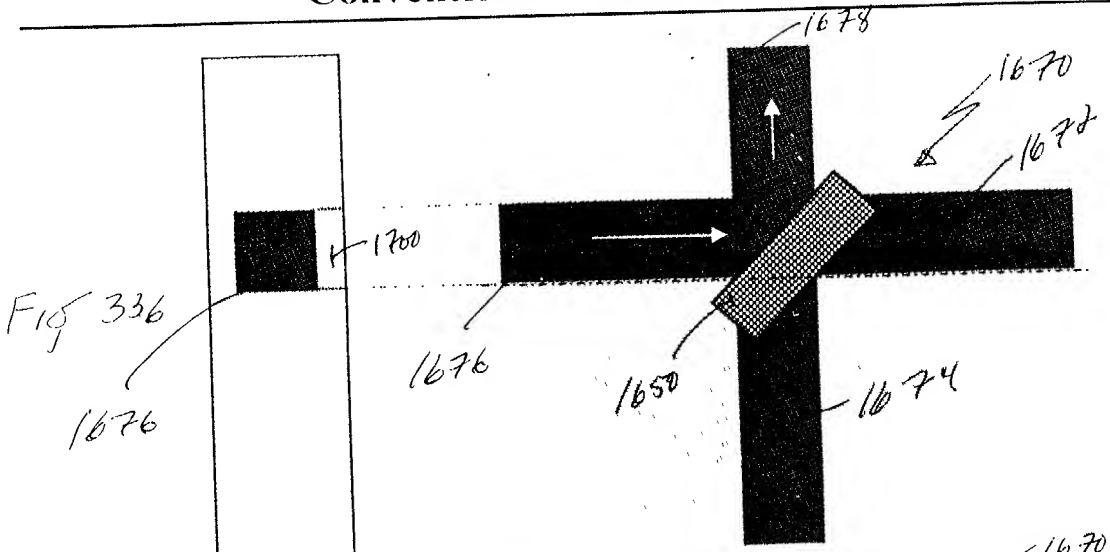

Fig 336

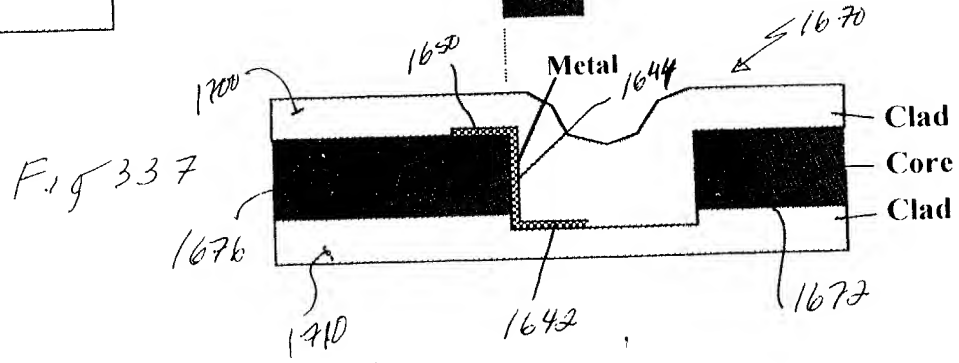

Fig 337

Invented Corner Turning Structure (I)

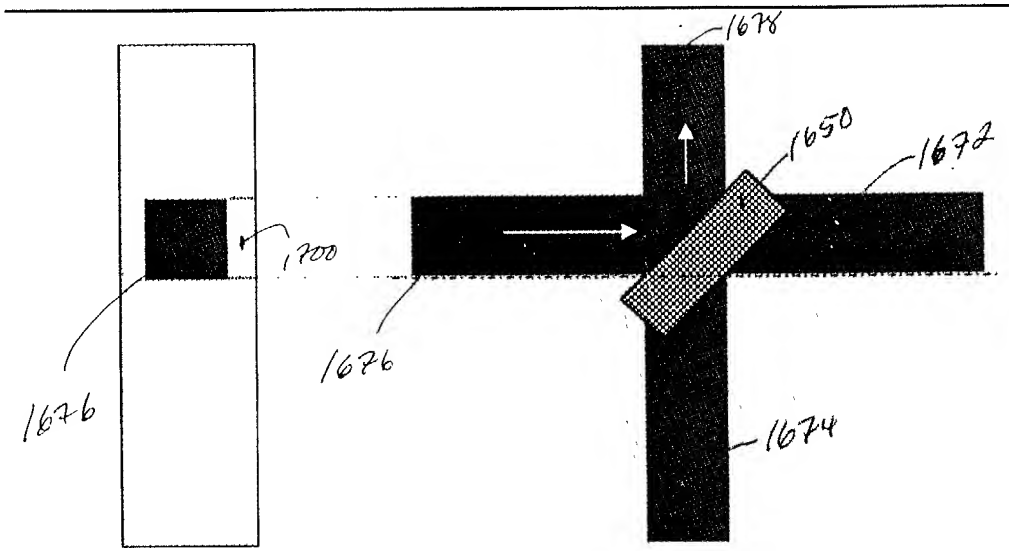

Fig 338

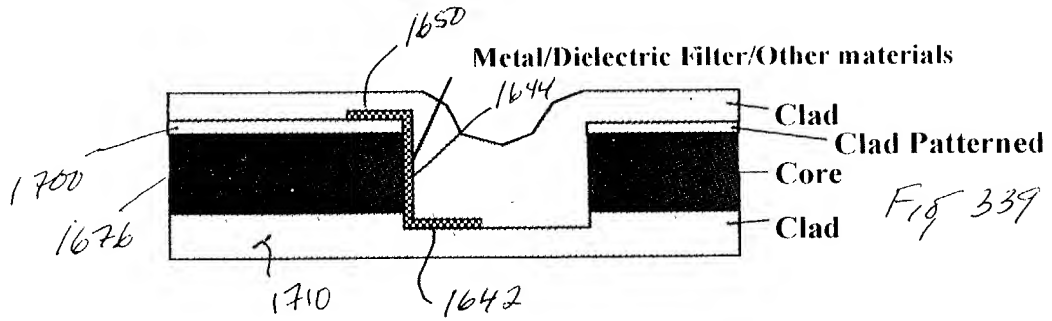

Fig 339

Invented Corner Turning Structure (II)

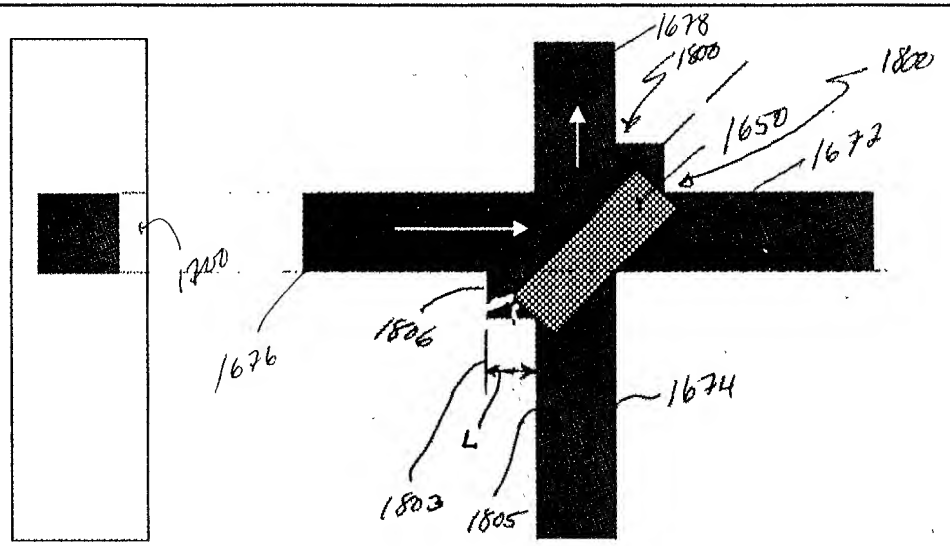

Fig 340

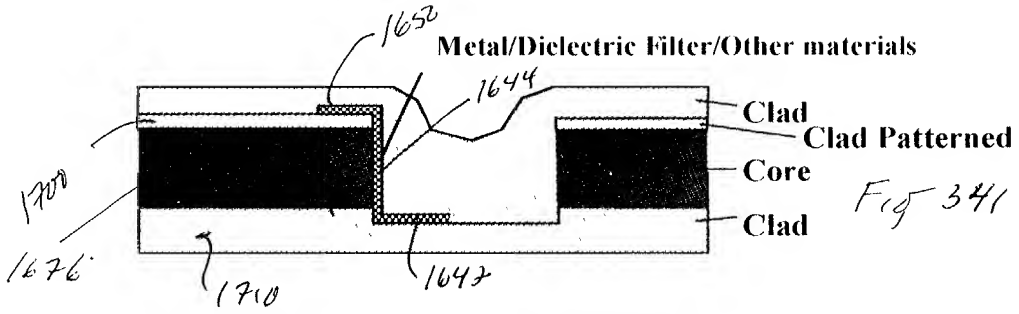

Fig 341

Conventional Coupler Structure (I)

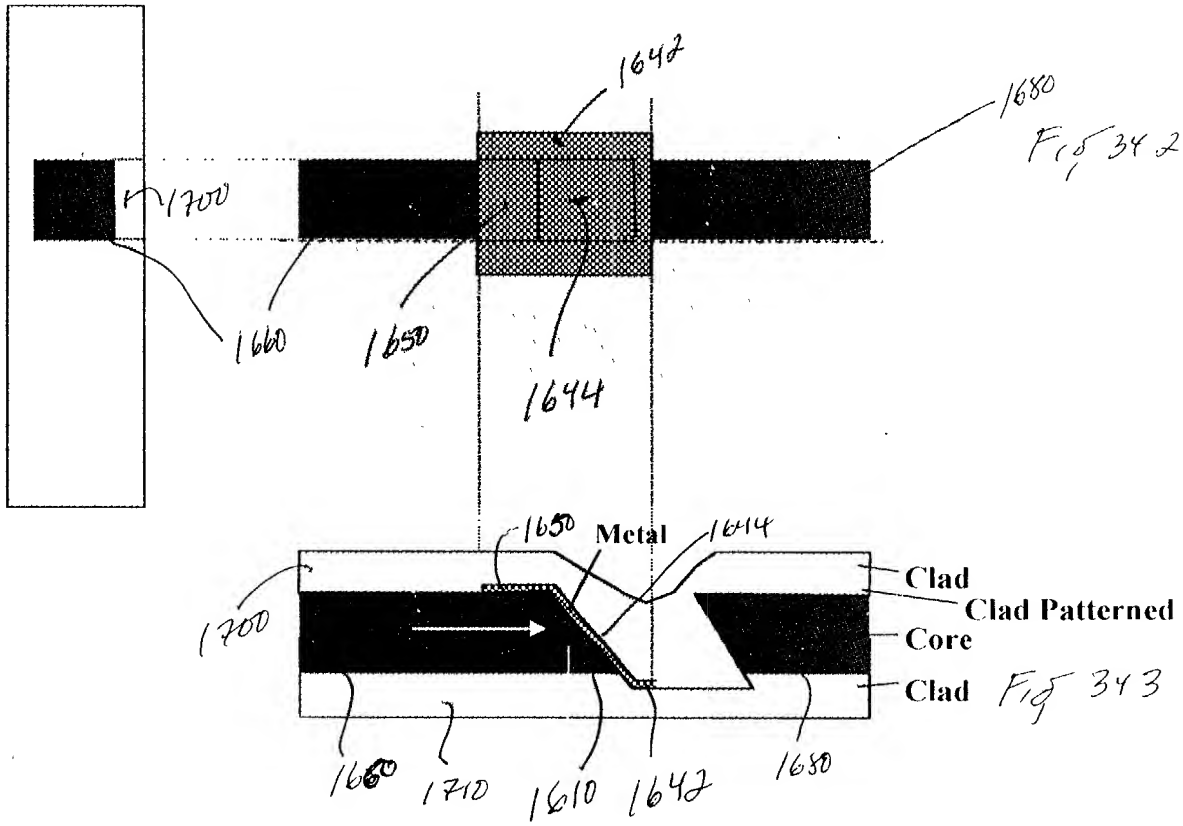

Fig 342

Fig 343

Invented Coupler Structure (I)

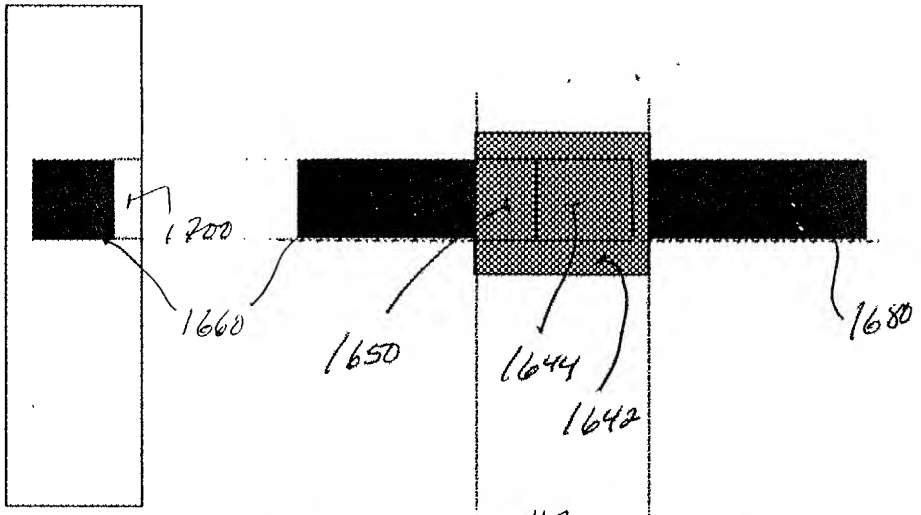

Fig 344

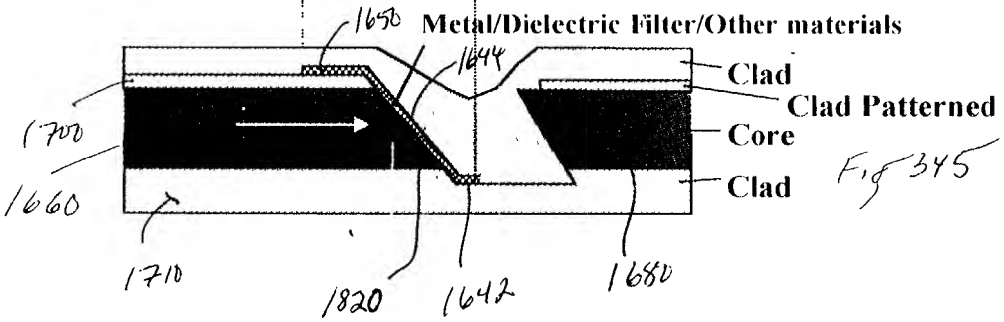

Fig 345

Invented Coupler Structure (II)

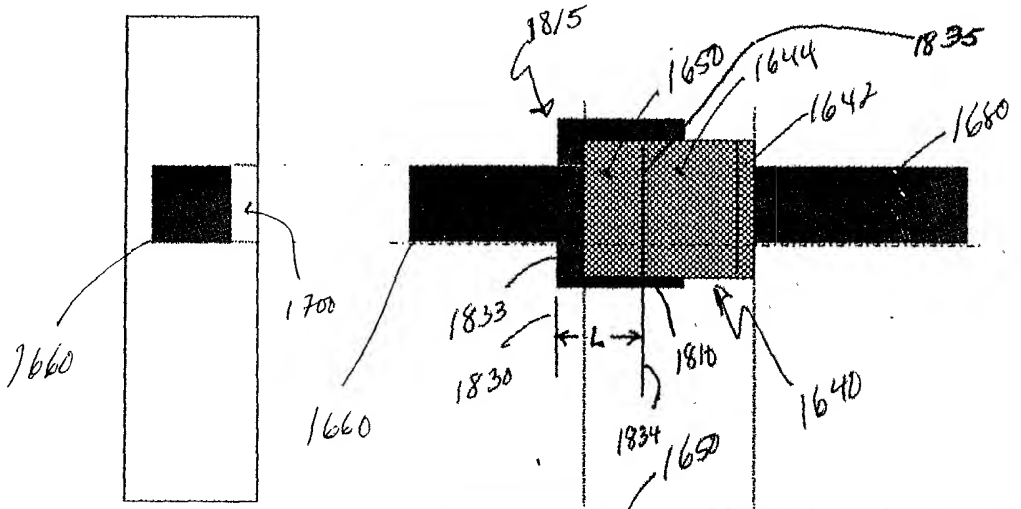

Fig 346

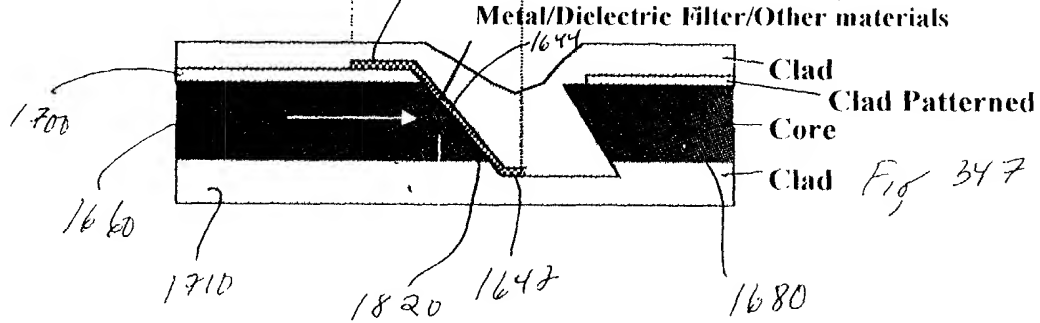

Fig 347

Excimer Laser Ablation Example for Beveled Cut (2)

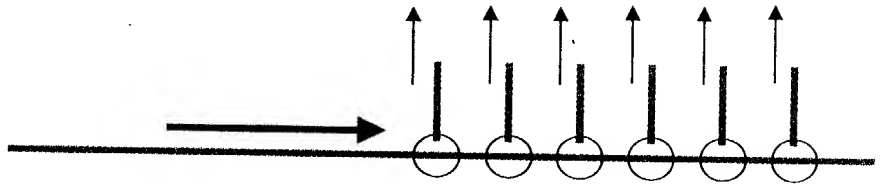

Fig 348

Beam Splitter

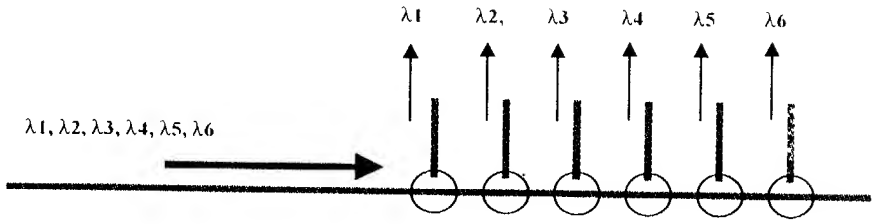

Fig 349

WDM DEMAX

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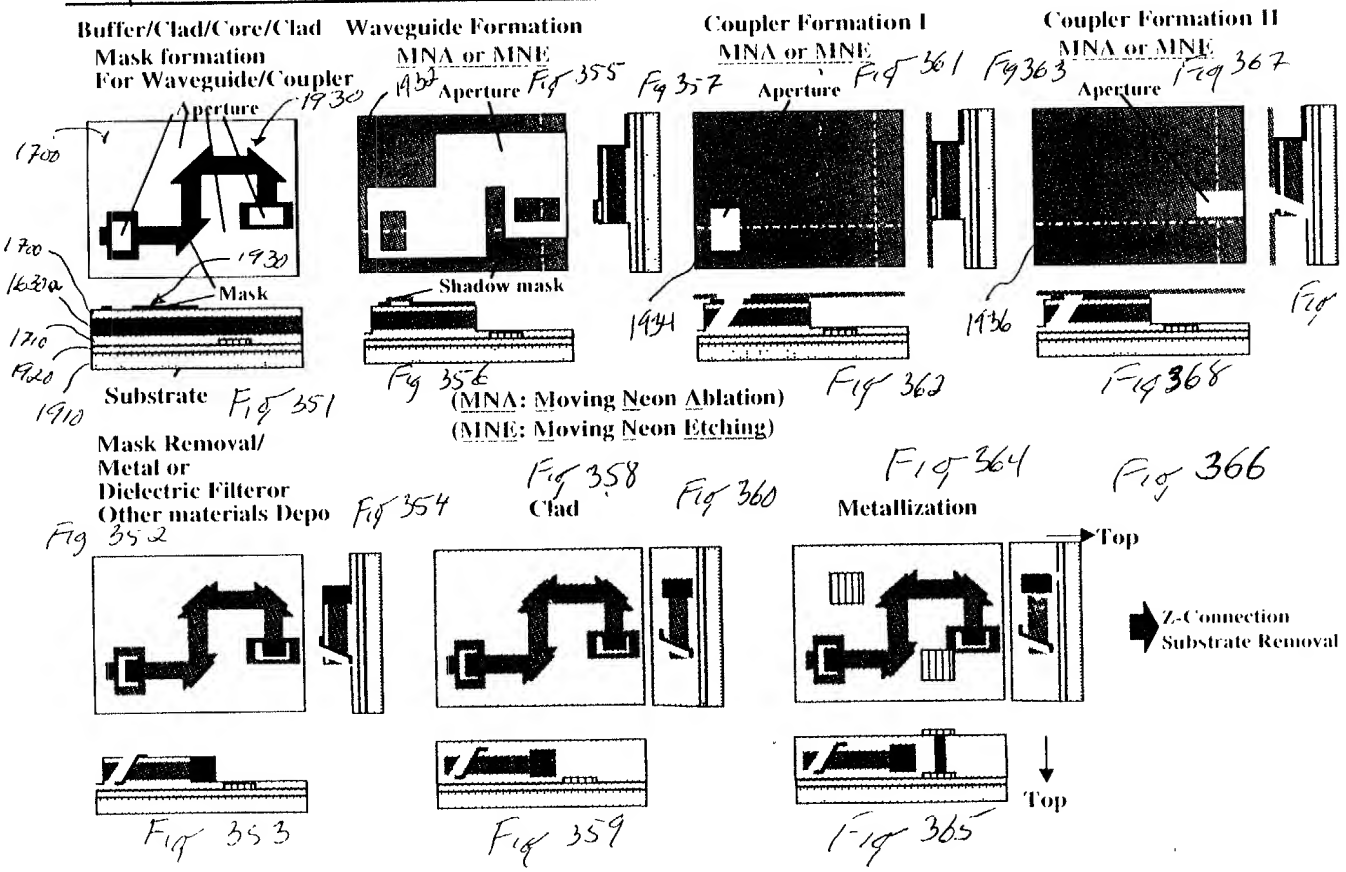
Fig 350

Another Process Flow for Structure (II)



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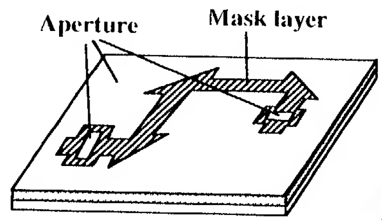
MNA, MNE Example for Add2 example

Fig 370



Excimer laser (or ion beam) with vertical incident angle

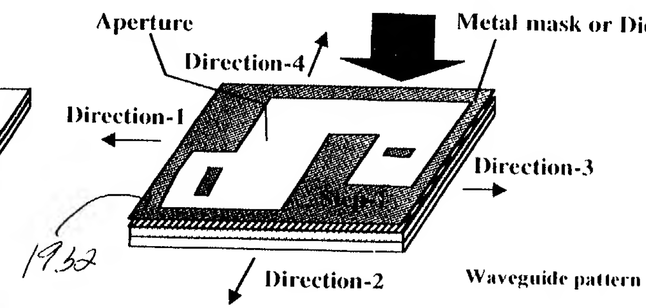


Fig 371

Excimer laser (or ion beam) with tilted incident angle

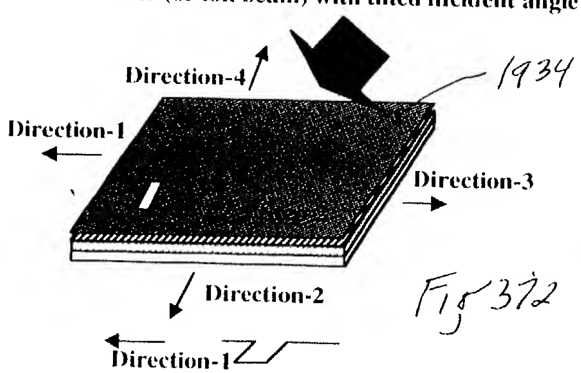


Fig 372

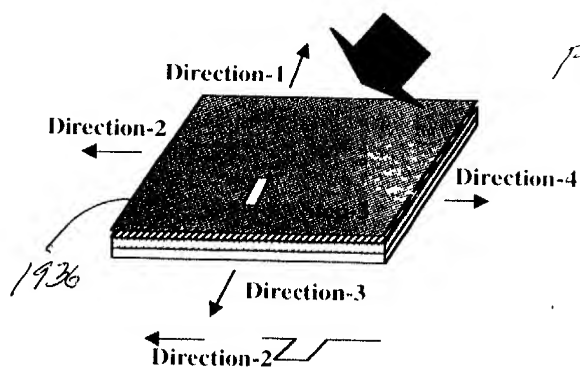


Fig 373

Invented Corner Turning Structure (A)

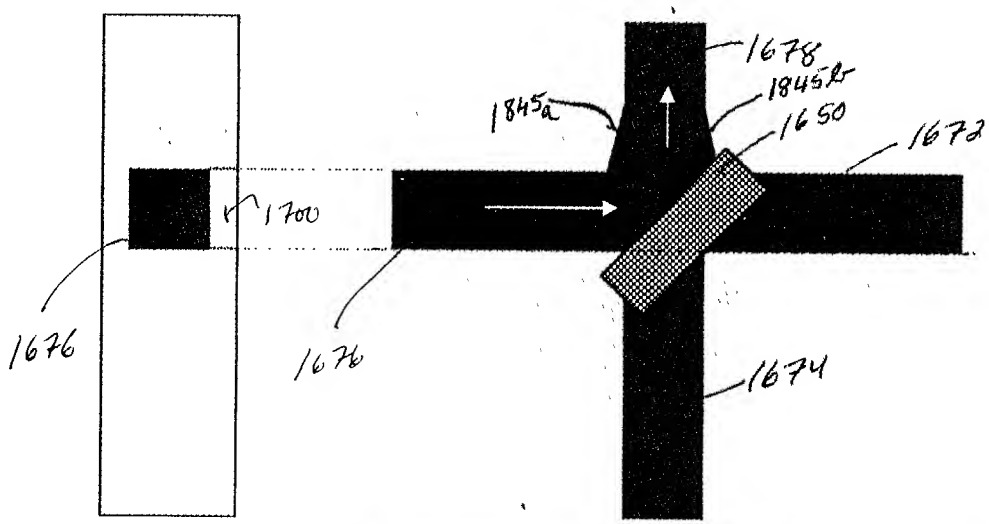


Fig 374

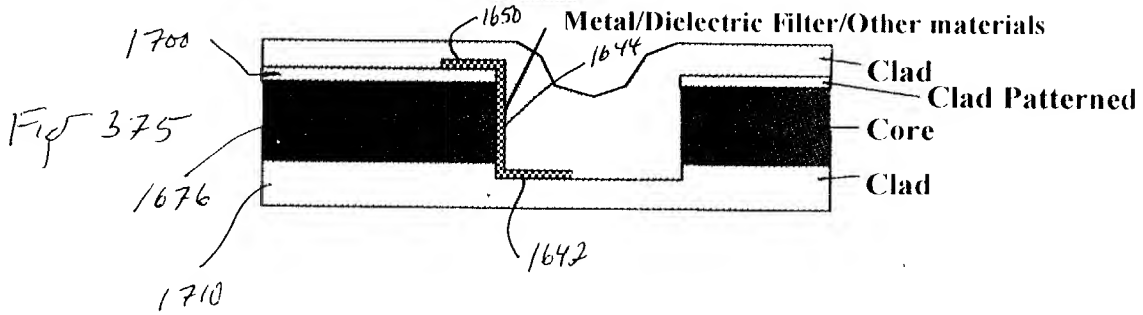


Fig 375

Example 3: Z waveguide Fab. Process 1

(a1) Metal pattern formation

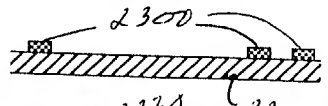


Fig 376

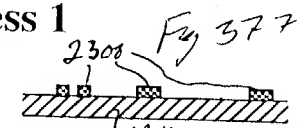


Fig 377

(a2) Core coat9
[DuPont, AlliedSig , ORMOCERs or F-PI]

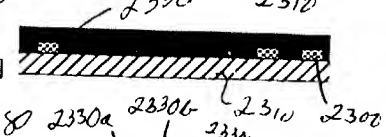


Fig 378

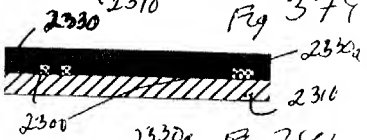


Fig 379

(a3) Z-WG core patterning
[UV-Exposure, mask-formation+RIE, Laser, or Dupont process]
Develpment
(for AlliedSig, ORMOCERs)

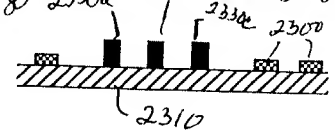


Fig 380

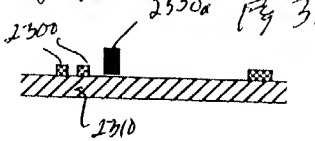


Fig 381

(a4) Clad coat
(for planarization viscosity adjust if necessary CMP)

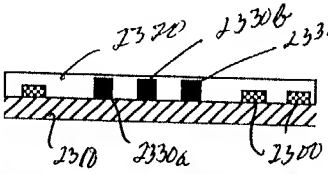


Fig 382

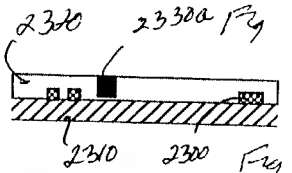


Fig 383

(a5) Core coat
[DuPont, AlliedSig , ORMOCERs or F-PI]

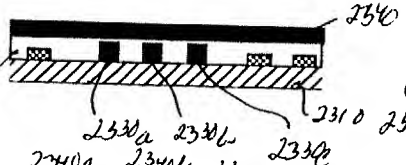


Fig 384

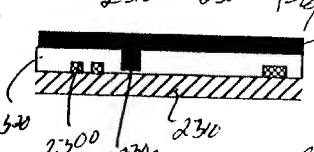


Fig 385

(a6) WG core patterning
[UV-Exposure, mask-formation+RIE, Laser, or Dupont process]
Develpment
(for AlliedSig, ORMOCERs)

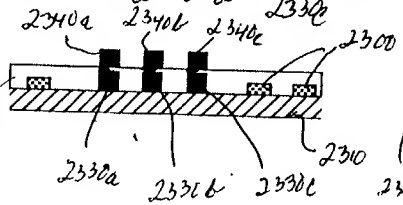


Fig 386

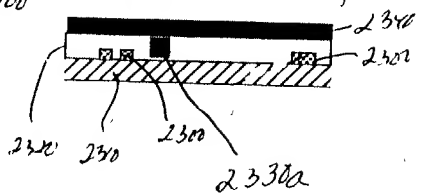


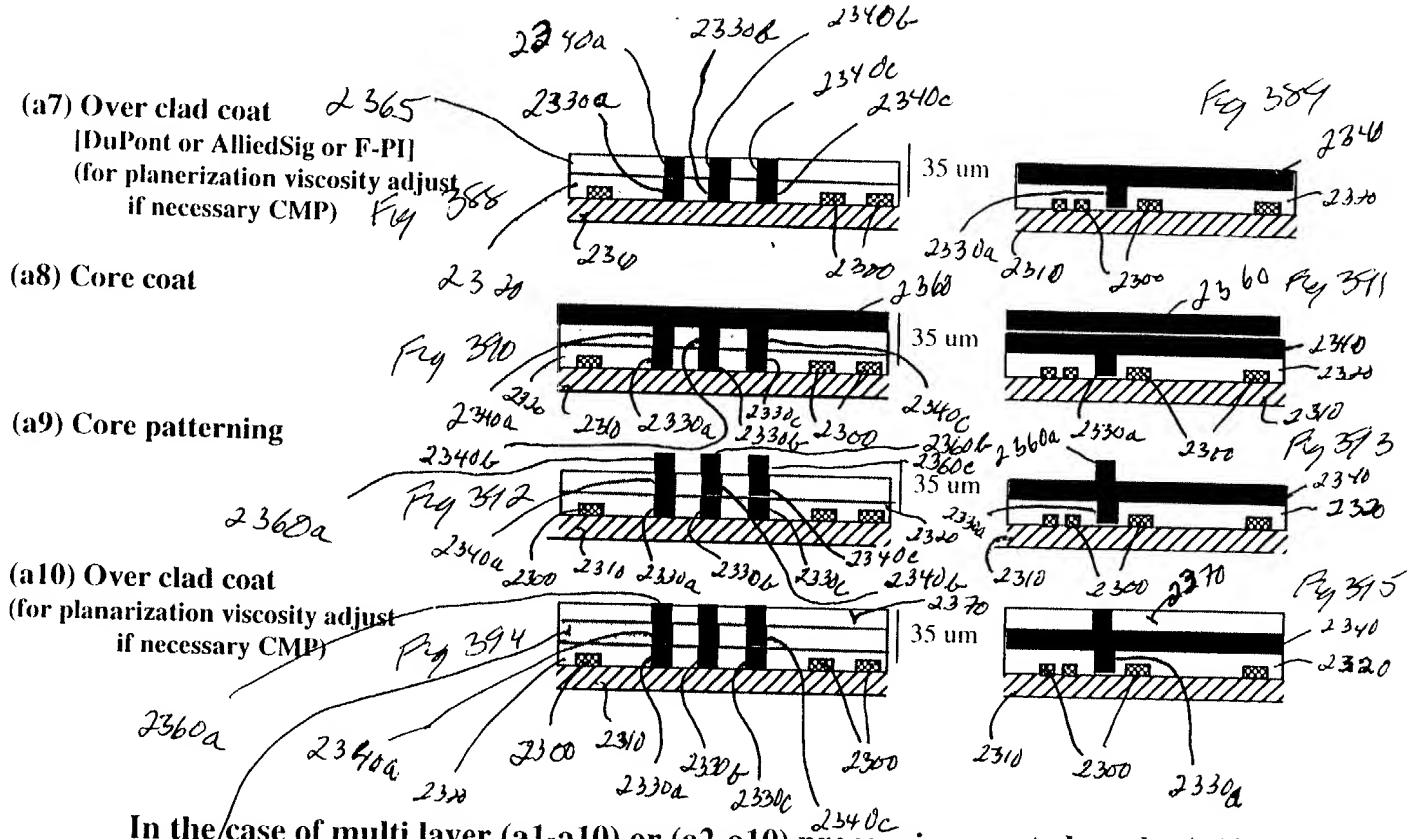
Fig 387

(a7) Over clad coat
[DuPont or AlliedSig or F-PI]
(for planerization viscosity adjust
if necessary CMP)

(a8) Core coat

(a9) Core patterning

(a10) Over clad coat
(for planarization viscosity adjust
if necessary CMP)



In the case of multi layer (a1-a10) or (a2-a10) process is repeated on the (a10).

Example 4: Z waveguide Fab. Process 2

(a1) Metal pattern formation Fig 396

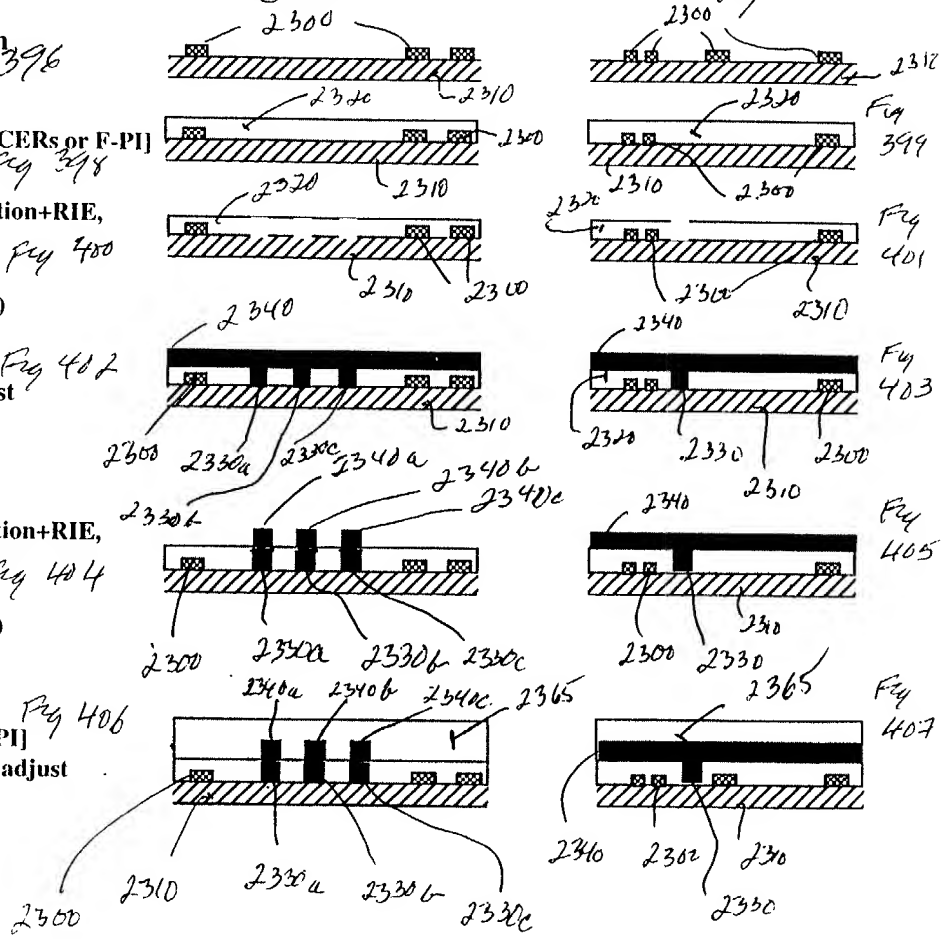
(a2) Clad coat
[DuPont, AlliedSig , ORMOCERs or F-PI] Fig 398

(a3) Clad patterning
[UV-Exposure, mask-formation+RIE, Laser or Dupont process] Fig 400
Develpment
(for AlliedSig, ORMOCERs)

(a4) Core coat Fig 402
(for planarization viscosity adjust if necessary CMP)

(a5) WG core patterning
[UV-Exposure, mask-formation+RIE, Laser or Dupont process] Fig 404
Develpment
(for AlliedSig, ORMOCERs)

(a6) Over clad coat Fig 406
[DuPont or AlliedSig or F-PI]
(for planerization viscosity adjust if necessary CMP)



(a7) Clad patterning
[UV-Exposure, mask-formation+RIE, Laser or Dupont process] Fig 408
Develpment
(for AlliedSig, ORMOCERs)

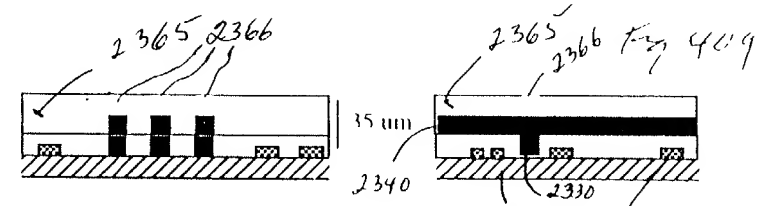


Fig 409

(a8) Core coat Fig 411
(for planarization viscosity adjust if necessary CMP)

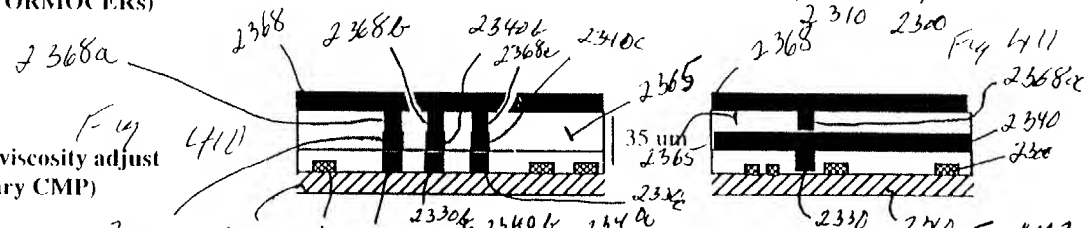
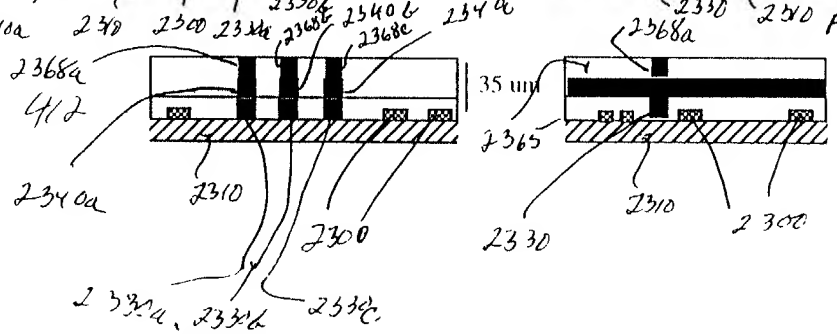


Fig 411

Fig 413

or

(a8) Core coat and CMP Fig 412



In the case of multi layer (a1, a5-a8) or (a5-a8) process is repeated on the (a8).

Fig. 414

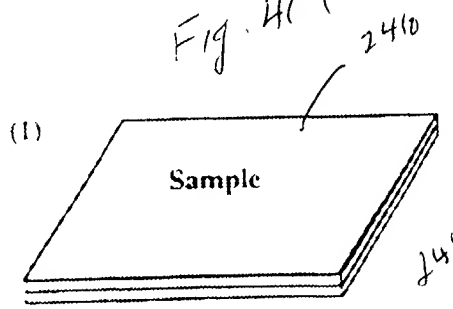


Fig. 415

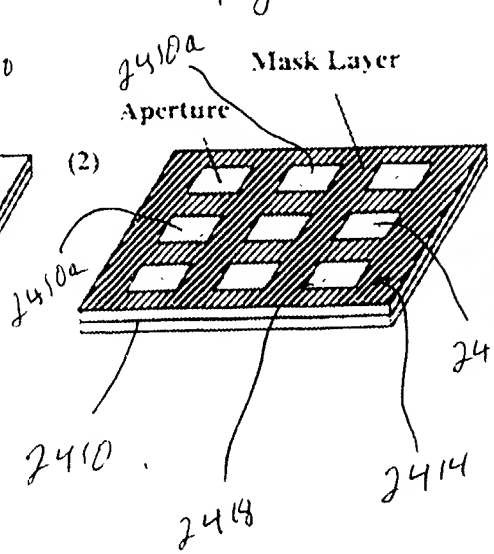


Fig. 416

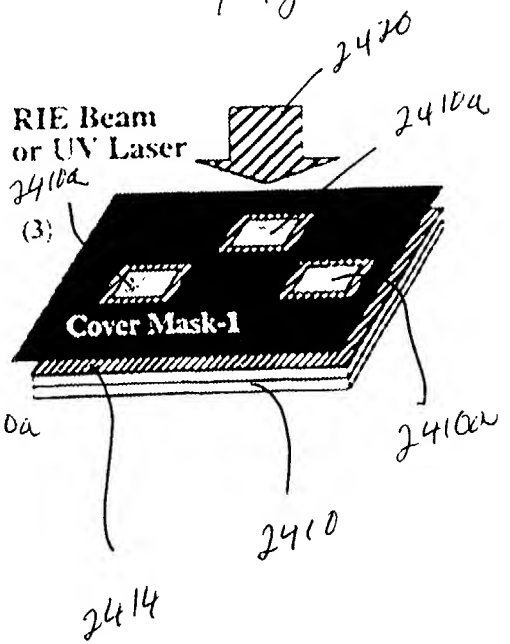
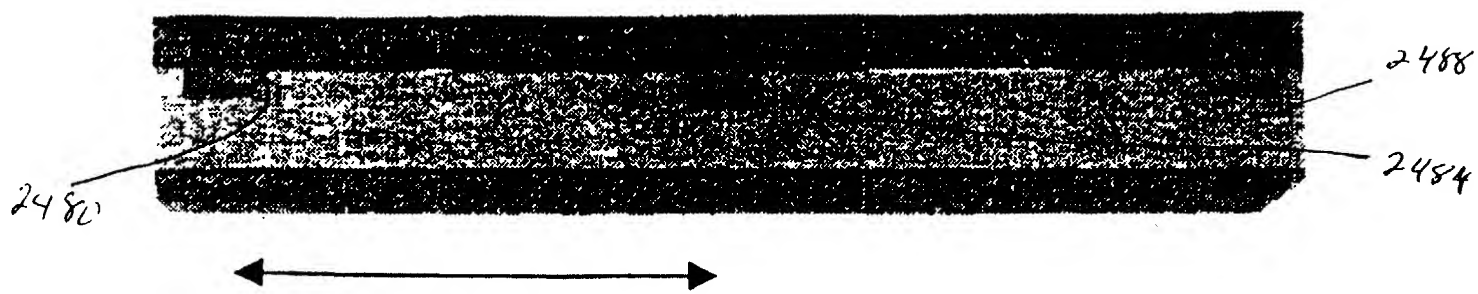
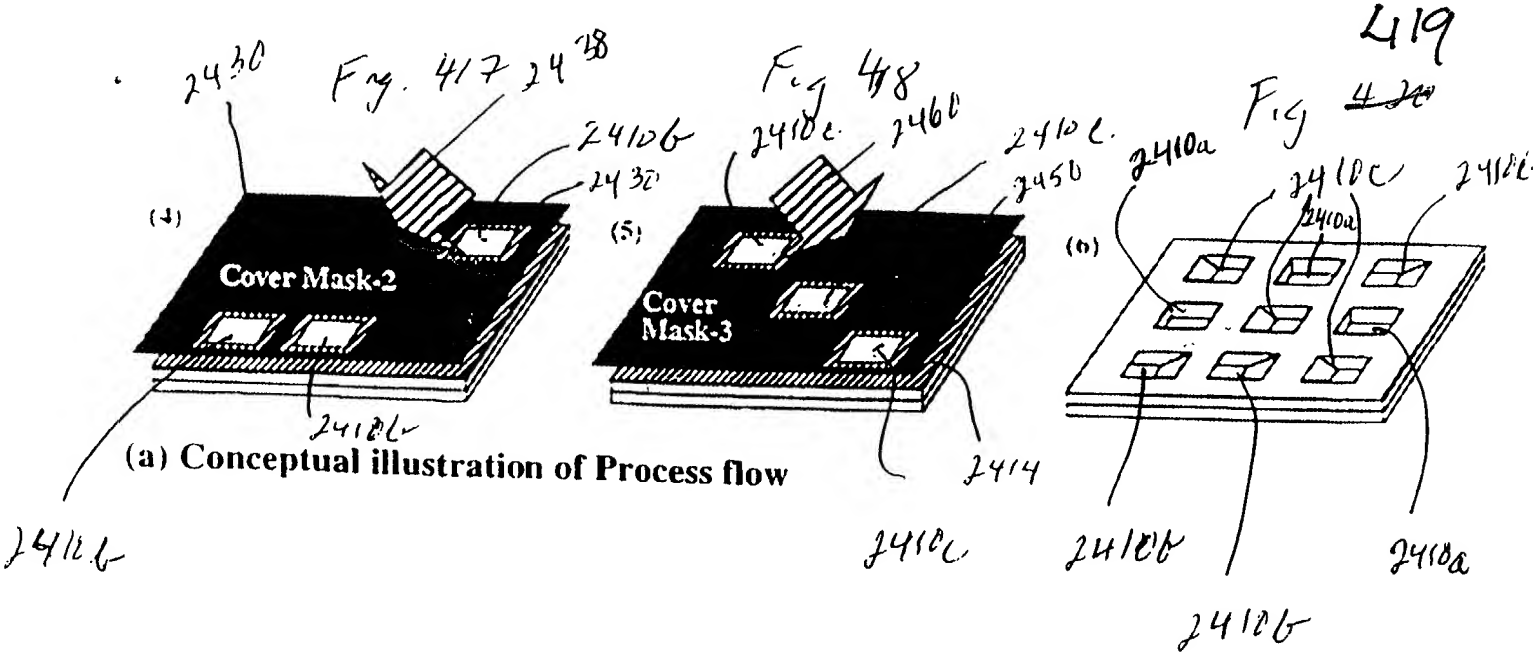


Fig. ~~4H~~ 420



(b) Trench wall formation of three different angles



(a) Conceptual illustration of Process flow

Fig. 417

Fig 418

Fig 419